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The 'HAMAC' rad-hard Switched Capacitor Array, a high dynamic range analog memory dedicated to ATLAS calorimeters.

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Abstract :

This note reviews the characteristics of the HAMAC analog memory designed for the read-out of the ATLAS calorimeters. It describes the circuit architecture, specifies its pin-out and gives simulated and measured performances. It also covers the radiation tolerance aspect.

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Modification / Draft 1

- PSRR simulation result (5.2)
- Adds on the test-setup description (6).
- Test on the V2 version of the DMILL chip (7).
- Tests on V2 chips with metallized backside (7).
- Gamma irradiation tests up to 300krad. (8)
- Neutron irradiation tests up to $1^{E}14$ N/cm^{2}. (8)
- Modifications planned on the pre-production prototype.

1 INTRODUCTION.

1.1 Introduction.

As described in the ATLAS calorimeter Technical Design Report (TDR) [1], the analog memory is located in the calorimeter read-out chain between the three-gain CR-RC2 shaper and the ADC. Its main function is to sample, at a 40 Mhz rate, the data coming from the shaper, to store them, waiting for the level-1 trigger decision, and then to send it slowly (5MHz) towards the ADC. For each trigger, the ADC will digitize 5 samples. As the system is supposed to present minimum dead time, the write operations will be unceasing even during the read phases. The chip can thus be seen as a simultaneous double random access analog memory array. The read and write addresses are generated by a separate controller chip [2] and send together with other control signals to the analog memory using low-voltage swings.

During the ten past years, several teams [3], [4], [5] have proven the feasibility of such analog memories, with dynamic range on the order of 12 bits, using S.C.A. (Switched Capacitors Array) structure. In those structures the analog memorisation is performed in capacitors addressed by CMOS switches. Two teams (Nevis and Orsay/Saclay) have then combined their experience to design a new circuit dedicated to the ATLAS calorimeter application.

1.2 Technology choice.

In the ATLAS experiment, the electronics will have to withstand a total ionising dose higher than 20 krad over a 10 year lifetime. For reliability, the circuit may survive to a total dose of 100krad. Thus the chip has been developed in two technologies : HP 1.2um CMOS non rad-hard technology and DMILL [6] [7] from TEMIC, a rad-hard BiCMOS technology, which is guaranteed by the vendor for 10 Mrad and 10^E14 N/cm^2 applications. The HP technology has been used for prototyping and for the realisation of batches needed for the module 0 of the calorimeter. The two chips are pin compatible, have the same architecture, and nearly (95%) the same schematics. Moreover, the technology available NPN is not used in the DMILL version. This DMILL chip is named HAMAC which stands for rad-Hard Analog Memory for Atlas Calorimeter. This note will described mainly this DMILL version.

1.3 Versions.

Three different versions of the chip have been submitted :

- V1, back in 1998. This version has been processed in two batches : 30 first samples (called V1.1) from the nominal batch and 30 extra samples (called V1.2) from a ‘backup’ batch have been tested.

- V2, submitted in December 1998. It includes anti-ESD protections on OUTM and OUTP outputs and a new addressing arrangement described in 7.12. It will allow to extend the statistics of the measurements and also to test the effects of a backside metallization (*). These chip will come back from packaging in June 1999.

- V3, submitted in June 1999. It is a mirrored version. The ‘MUON’ mode is available only on this new version. It uses the standard addressing arrangement.

(*) metallization of the backside realised on DMILL front-end chips, based on S.C.A. structures, designeded to ATLAS trackers, improve fixed sequence noise performances by a factor of 2 [10]

CHIP VERSION	BATCH ID.	LOGO ON THE CHIP	PACKAGE MARKING	DELIVERY	MIRRORED	BACKSIDE METALLIZED	MUON mode available
V1	V1.1	HAMAC	HAMAC DMILL E1 or E2	June 98	No	No	No
V1	V1.2	HAMAC	HAMAC DMILL E3	Aug 98	No	No	No
V2	V2 Waf 12	HAMACM	HAMAC DMILL E4	June 99	No	No	No
V2	V2 Waf 4	HAMACM	HAMAC DMILL E5	Aug 99	No	Yes	No
V2	V2 Waf 4M	HAMACM	HAMACM DMILL E5M	Aug 99	Yes (packaged upside-down)	Yes	No
V3		CAMAH		Oct 99	Yes (layout)	?	Yes

2. CIRCUIT DESCRIPTION

2.1 General description and requirements. Normal and mirrored versions.

Fig 1 shows the architecture of an 8-channel elementary block of the front-end board. One 5 MHz ADC is shared between two SCAs, the multiplexing between the both being described in 2.3.4.

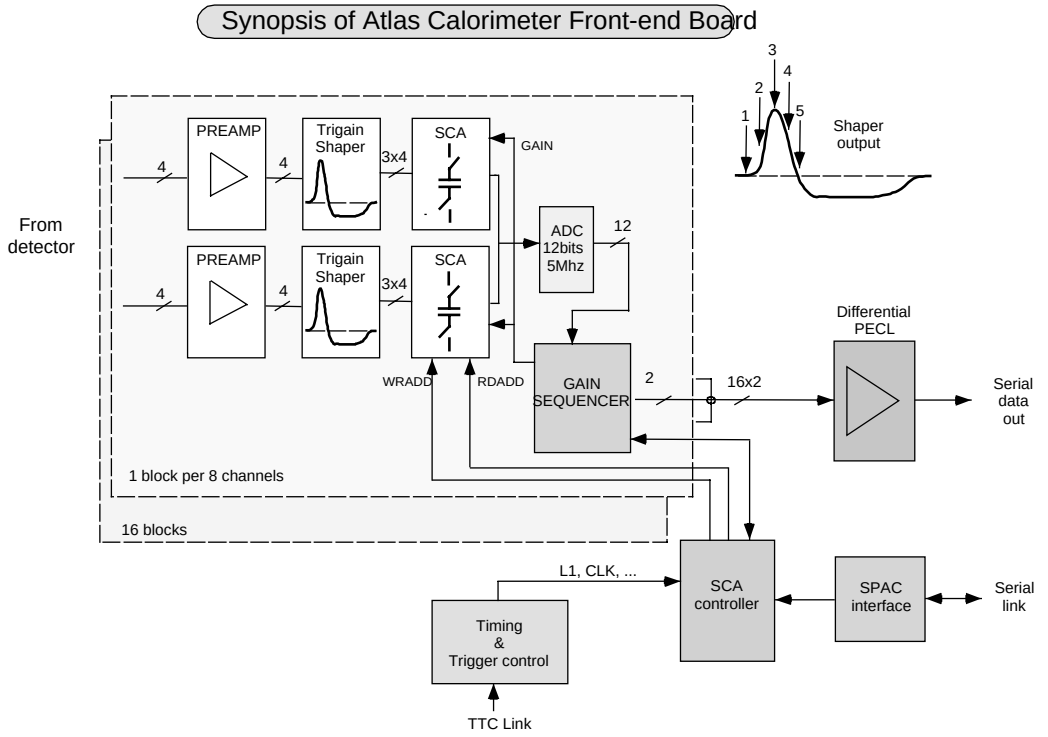


Fig 1 : Block diagram of the calorimeter front-end board

The signals coming out of the shapers are sent to the analog memories. Inside each memory, the signals are sampled at 40 MHz and stored until the SCA controller receives a level 1 trigger. Then the five samples

corresponding to the selected event will be driven sequentially towards the output of the chips. At this point and for each sample, the 2x4 internal channels of two associated chips are multiplexed at a 5 MHz rate.

For each channel, the peak sample (the third sample) is first read. It is compared on the medium gain both to saturation and to a low threshold. Depending on the result of the comparison, one of the gains is chosen and stored. Then the same sample is read once again on the right gain, and sent to the output. All the four other samples are also read on the same gain as the peak sample. The total time needed for reading a group of 8 channels with 5 samples is thus 9us.

Due to space constraints, the two SCAs inside the same 8 channel-group will be located each on a side of the Front End Board (F.E.B). To allow the sharing of their command and address lines using a straightforward layout, the two chips have a different pinout. **In fact, two different chips should be produced : the standard one and a mirrored one obtained from the latter by an axial symmetry of the layout (*).** The parity signal (M) indicates which one of the two SCAs is the first multiplexed towards the ADC .

Each gain of the four calorimeter channels filtered inside a shaper chip is stored in a pipeline channel. An extra slave channel is associated with each group of three gains corresponding to a calorimeter channel. The inputs of the four slave channels are connected together to the reference output of the shaper. The slave channel will be treated by the SCA exactly as the other channels and its output will be subtracted to the signal output during the read operation. This subtraction is performed off-chip. This pseudo-differential operation is supposed to reject the major part of the coherent noise generated before and inside the chip such as clock feedthrough and couplings through the substrate. It also improves the power supplies rejection ratio (PSRR) of the chip.

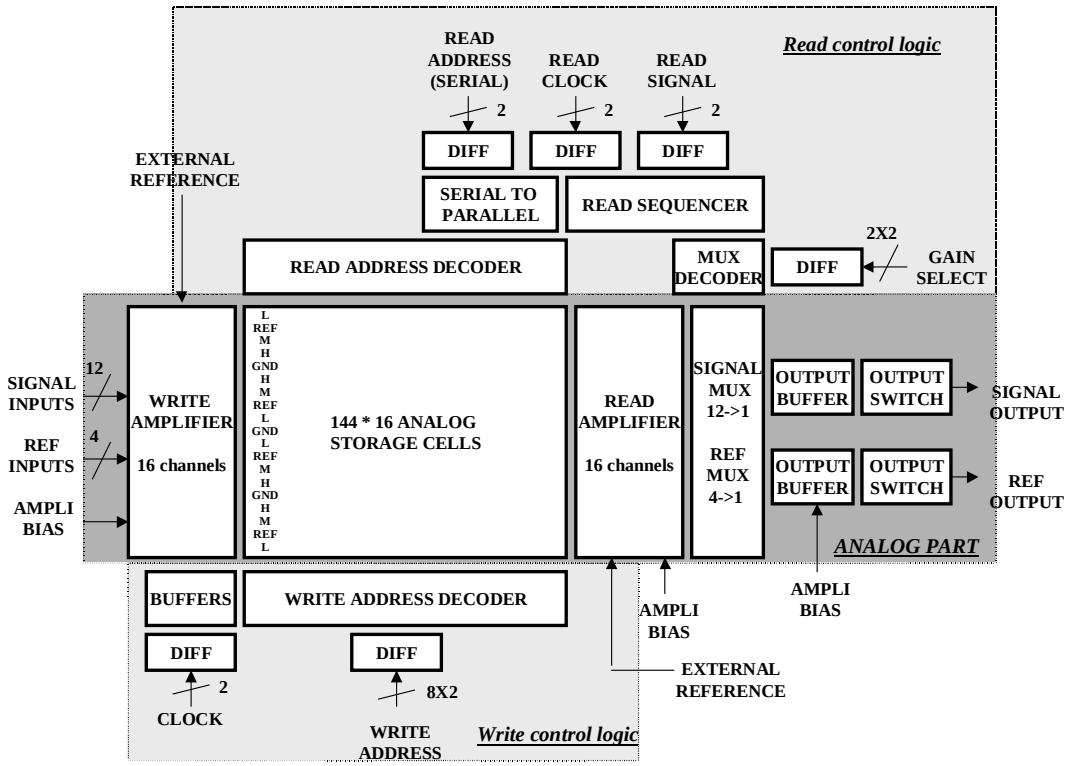


Fig 2 : SCA main building blocks

(*) An other way to produce the mirrored chip from the normal one by turning it upside-down during the packaging operation is under investigation.

Due to these four extra channels, the chip consists of 16 storage channels of 144 cells each. The cell number is set by the maximum trigger rate, the trigger latency and the number of 5 samples kept per event [8]. The output of the shaper is DC coupled to the input of the SCA. As a result, the SCA is asymmetrically powered (VSS=-1.7V, VDD=+3.3V) to deal with input signals in the range of –0.9V/+2.5V with a baseline voltage of 0V.

Fig 2 shows the internal building blocks of the SCA. They can be divided in three groups :

- the analog part described in section 2.2.
- the digital write part described in section 2.3.1
- the digital read part in section 2.3.2

2.2 Analog part

Each of the 16 channels of the chip (Fig 3) consists in :

- A write buffer section including input buffers for both the write and return busses.
- A bank of 144 storage cells.
- A read amplifier.

The 16 channels are multiplexed towards the two output buffers which drive the two output pins.

2.2.1 Input pins arrangement.

As signals with very different amplitudes are treated simultaneously by the SCA, the crosstalk within and at the input of the chip needs to be minimized. One possible source of crosstalk could be the capacitive coupling between adjacent input pins of the package. For this reason, the following input pin arrangement has been chosen :

Low GAIN CHANNEL 4
Slave CHANNEL 4
Medium GAIN CHANNEL 4
High GAIN CHANNEL 4
GND
High GAIN CHANNEL 3
Medium GAIN CHANNEL 3
Slave CHANNEL 3
Low GAIN CHANNEL3
GND
Low GAIN CHANNEL 2
Slave CHANNEL 2
Medium GAIN CHANNEL 2
High GAIN CHANNEL 2
GND
High GAIN CHANNEL 1
Medium GAIN CHANNEL 1
Slave CHANNEL 1
Low GAIN CHANNEL1

High gain (potentially treating large or saturated signals) and low gain inputs are always separated by two pins including a ground or slave channel pin. Input pins corresponding to different calorimeter cells are always separated by at least one grounded pin.

2.2.2 Memory cell.

The storage cell (see Fig 3) is composed of four switches and one capacitor. S1 and S3 which have to deal with the input signal dynamic range are CMOS switches whereas S2 and S4 are simple NMOS switches as they are connected to a fixed intermediate level.

During the write operation, S1 and S2 are closed and the voltage across the capacitor tracks the difference of voltage between the write bus and the return bus : this is the tracking period.

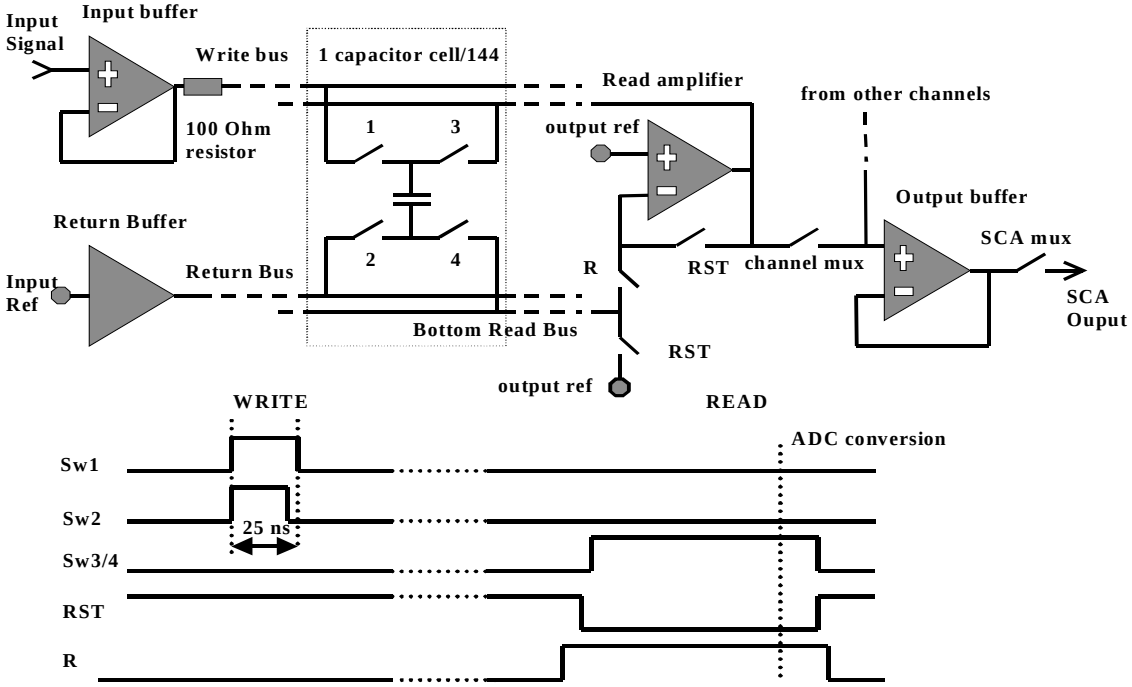


Fig 3 : SCA channel architecture and write and read sequences

S2 and the NMOS switch are opened at the same time while the PMOS of S1 is kept closed. Thus only S2 performs the real sampling. As S2 is connected to a quasi invariant voltage (the return bus), both the time of the sampling and the charge injected into the capacitor during the operation are kept independent of the signal value, thus avoiding undesirable non-linearity. The PMOS of S1 is turned off a couple of ns later.

To achieve the best settling time accuracy, the tracking period duration Ttrack must be as long as possible inside a 25ns write period. However, to avoid the perturbation due to the switching on of a new storage cell on the write busses, it is important to close the write switches only after those of the previous written cell have been opened. All the timing of the switch commands are then carefully generated in the digital write part. The typical duration of Ttrack will be of 23ns.

To be read back, the Cs capacitor will be put in the feedback of the read amplifier by closing S3 and S4 after the read bottom bus has been reset (see section 2.2.4).

As the write and read operations are both performed in voltage mode, the gain of the chain, very close to 1, is at first order independent of the value of Cs.

In order to reduce the sensitivity to the noise injected in the chip back silicon, the top plate of the storage capacitor is the one connected to the sensitive input node of the read amplifier during the read operation whereas the bottom plate which presents a parasitic capacitance to back silicon is the one connected to the output of this amplifier.

If the 1/f noise is ignored, the total output-refered rms noise voltage of **one** SCA channel can be expressed as :

(1) $\langle vch^2 \rangle = ei^2 * Bwi * \pi/2 + kT/Cs + kT/Cs * Cp/Cs + ((Cp+Cs)/Cs)^2 * er^2 * Bwr * \pi/2 + eb^2 * Bwr * \pi/2$

(**this expression is doubled by the differential operation**).

where : ei is the input buffer voltage power spectral density referred to the channel input.
er is the read amplifier voltage power spectral density referred to its input.
eb is the output buffer voltage power spectral density referred to its input.
Bwi is the –3dB bandwidth of the amplifier + cell section.
Bwr is the output circuit –3dB bandwidth (eventually including a low pass external filter).
Cs is the value of the storage capacitance.
Cp is the capacitance of the bottom read bus.

The first term corresponds to the sampling of the input buffer noise. The second term represents the noise of S2 sampled on Cs. The third term corresponding to the reset of the bottom read bus will be explained in 2.2.4. The 4^{th} and 5^{th} terms correspond to the noise, eventually filtered off-chip, respectively of the read amplifier and the output buffer.

The charge injection, the clock feedthrough and their cell-to-cell dispersion scale at first order as 1/Cs.

Therefore the value of Cs has to be maximised to minimise both the noise and the charge injection dispersion.

Conversely, the storage cell time constant :

(2) $\tau s=(Ron(S1) + Ron(S2)) * Cs$ (where Ron(S) is the switch equivalent resistance)

needs to be smaller than Ttrack/9 to achieve a settling precision of 13 bits.

A large capacitor will also be more difficult to drive by the input buffers. The **1pF value chosen for Cs** results from a trade-off between these numerous constraints.

The sizing of S1 and S2 leads to a typical τs=2ns corresponding to a BWc= 80MHz bandwidth, while maintaining S2 (main source of the charge injection during the sampling) as small as possible.

The 4^{th} term of equation (1) scales as the value of Cp. As the bottom read bus is drawn using the minimum drawing rules, Cp is dominated by the drain-bulk and drain-gate overlap capacitance of M4 switches. In consequence, S4 is a minimum size transistor.

S3 sizing is principally driven by the read-out speed constraint.

The memory cells are as narrow (26um*200um) as possible to minimise the length of the read and write busses but also to obtain a square shape easier to package. The differential write and read commands are bussed in metal2 across the storage capacitor, but a metal1 shield screens the coupling between this line and the top plate of the capacitor.

To limit crosstalk, a 50µm empty space has been kept free between the channels.

2.2.3 Input buffers.

At the input of a channel, the shaper output is buffered by a write amplifier which drives the top write bus. The aim of this buffer is to limit the voltage of the input signal, to present a constantly low capacitive load to the shaper output and to decrease drastically the level of crosstalk by buffering the flow of signal currents on and off the chip, what has proven to be the major source of crosstalk.

This buffer is an operational amplifier connected as a voltage follower (output connected to its negative input).

Its open loop structure (Fig4) with a pseudo class A output stage allows the high slew rate capability (150V/us) needed for the application. For rising edges, the slew rate is limited by the charge of the N1 node. For falling edges, it is limited by the charge of the output node capacitance by the current delivered by M9. In this structure, this current is modulated by the input signal via M4-M5 and M8-M9 current mirrors. It can be increase by a factor of two in case of falling edges, improving then the negative slew-rate by the same factor without any power consumption penalty .

The two gain stage structure allows to reach DC open-loop gain higher than 60dB and allows a 'lead' compensation (Mc, Cc).

The sizing of the amplifier transistors and compensation network has been performed to ensure a perfect stable operation with a –3dB bandwidth of 80 MHz and a low noise. This noise, simulated as 70uV rms referred to the input of the amplifier, is dominated by the contribution of the input pair M1,M2, and is essentially high frequency noise. To keep it as small as possible, large width and non-minimum gate length has been chosen for M1 and M2 580um/1.2um).

The amplifier currents are defined by the current flowing in the M10 transistor. The IPOL nodes of the 16 amplifiers are connected together so that the bias current is defined via an external resistor connected between this common node and VDD.

The systematic offset, as it is supposed to be corrected by the differential operation, was not a design or a layout criterion.

To ensure a very stable operation, a small value P+ diffusion resistor (100 Ohm) is put in series between the amplifier output and the write top bus.

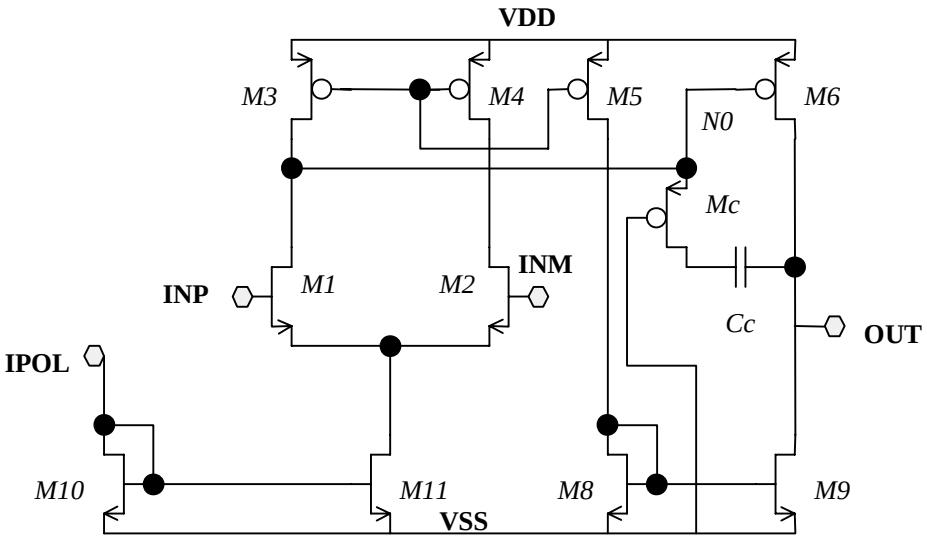


Fig 4 : open-loop structure of the pseudo class A amplifier

Similarly, an other buffer, connected to the return bus, reduces cross-talks by limiting the currents coming from the common reference pin of the chip, what could produce common mode voltage changes on the return busses.

This buffer needs essentially a high input impedance and low output impedance without wide dynamic range requirement. A simple NMOS source-follower is used for this purpose. The common input reference voltage of these 16 followers is generated by a servo-control system (Fig 5) which sets the write return bus voltage to VREF.

The total static power consumption of the write amplifier section is 9.5mW/channel for a typical case of process:

- 500uW for the biasing branch.
- 3mW for the source follower.
- 6mW for the input buffer.

As the current needed in the write section are high (30.5mA in the power supplies), the power supplies lines are large (50 um wide) metal 2 lines to limit both electromigration and voltage drops. The common IPOL line is a 30um wide metal2 line.

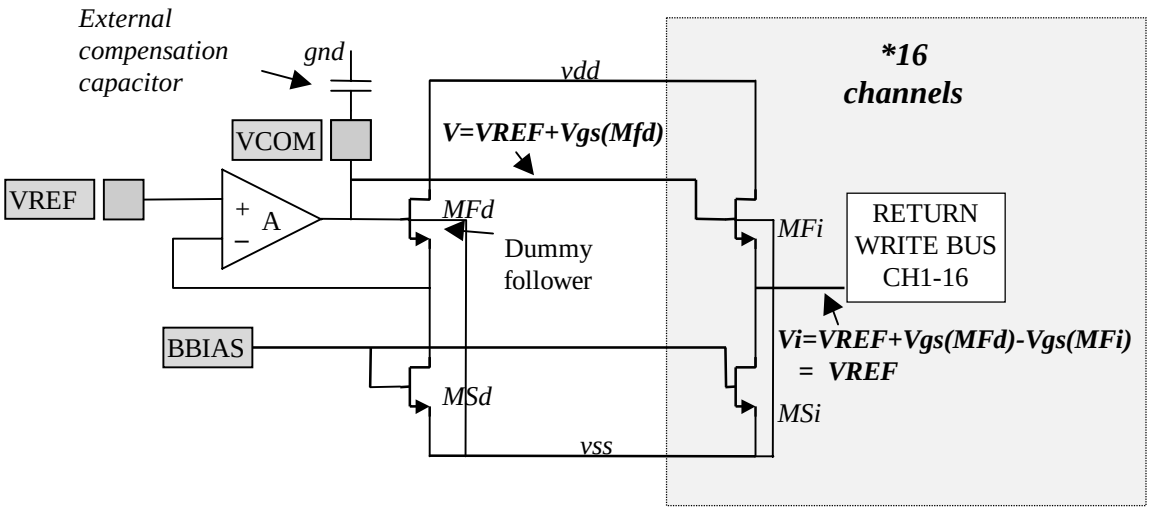


Fig 5: return bus followers and servo-control structure

2.2.4 Read amplifiers and reset switches.

The read amplifier has the same open-loop structure as the write amplifier but uses a PMOS transistor input pair. Indeed, this type of transistor is preferred for its lower white and 1/f noise.

The sizing of the transistors and of the compensation network have been driven by the low noise (dominated by the large 160um/1.2um input transistors) requirement and the stability constraints during the reset ande read-out phases.

Before reading a capacitor, the residual charge stored on the parasitic capacitance of the bottom read bus needs to be cleared to avoid the mixing of two consecutive signals : this is the purpose of the reset phase. During this phase, the RST switches are closed, setting the read amplifier in voltage follower mode and discharging the bottom read bus, while R is opened insulating the read amplifier input from the bottom read bus capacitance to avoid oscillations. This phase lasts at least 100ns to allow discharging of the bottom read bus with a sufficient precision.

At the end of the reset phase, the RST switches are opened just before that R be closed. The squared rms value of the noise sampled on the read bottom bus at this critical time is :

(3) $\langle vbus^2 \rangle = kT/Cp + (kT/Cra + \langle vnra^2 \rangle) * (Cra/(Cp+Cra))^2$

where :

- Cp is the value of the bottom read bus capacitance.
- Cra is the value of the read amplifier input capacitance.
- vnra is the input-refered noise voltage of the read amplifier .

As Cra<<Cp , (4) $\langle vbus^2 \rangle = kT/Cp$.

At this moment, the read amplifier is ready to read back a storage capacitance. To do this, the capacitor is mounted across the read amplifier. During this read phase, the noise contribution expressed in (4) is amplified by the voltage gain of the amplifier which is defined by Cp/Cs in this and becomes :

(5) $\langle vbusout^2 \rangle * (Cp/Cs)^2 = kT/Cs * Cp/Cs$ at the output of the amplifier, which is the 3rd term of the expression (1).

In practice, this contribution remains small, but it can not be filtered by off-chip external filters.

One can notice that, by the same mechanism s, every voltage sampled on the bottom read bus at the end of the reset operation will be multiplied by the Cp/Cs ratio. This is true as well for the pickup generated by digital signals as for the charge injected by the local switches. It will result in :

- channel-to-channel offsets if the perturbations are independent on the addresses.
- fixed sequence noise if the perturbations are address-dependent.

The white noise of the read amplifier is also amplified by a voltage gain (defined here by (1+Cp/Cs)) . Its rms value at the output of a channel can be expressed as :

(6) $\langle vra^2 \rangle = ((Cp+Cs)/Cs)^2 * er^2 * Bwr * \pi/2$ which is the 4th term of the expression (1).

In practice, this contribution appears as the main one. It can be reduced by decreasing the read-out bandwidth.

As the 13-bit precision settling time of the read amplifier output signal is 125ns, the output multiplexing and digitisation can begin one read clock period (200ns) after the end of the reset operation.

As for the input buffer, the read-amplifiers bias currents is defined by an external resistor.
The static power consumption of each read amplifier is 3.8mW including the bias branch.

2.2.5 Channel multiplexer, output buffer and SCA multiplexer.

At the output of the read amplifiers, the 12 signal channel outputs are multiplexed by CMOS switches towards the signal output buffer. In the same way, the 4 slave channels are multiplexed towards the slave output buffer. The commands of the switches are generated by a sequencer within the digital read-out part. When no channel is selected, the inputs of the two output buffers are clamped by PMOS transistors to a reference voltage.

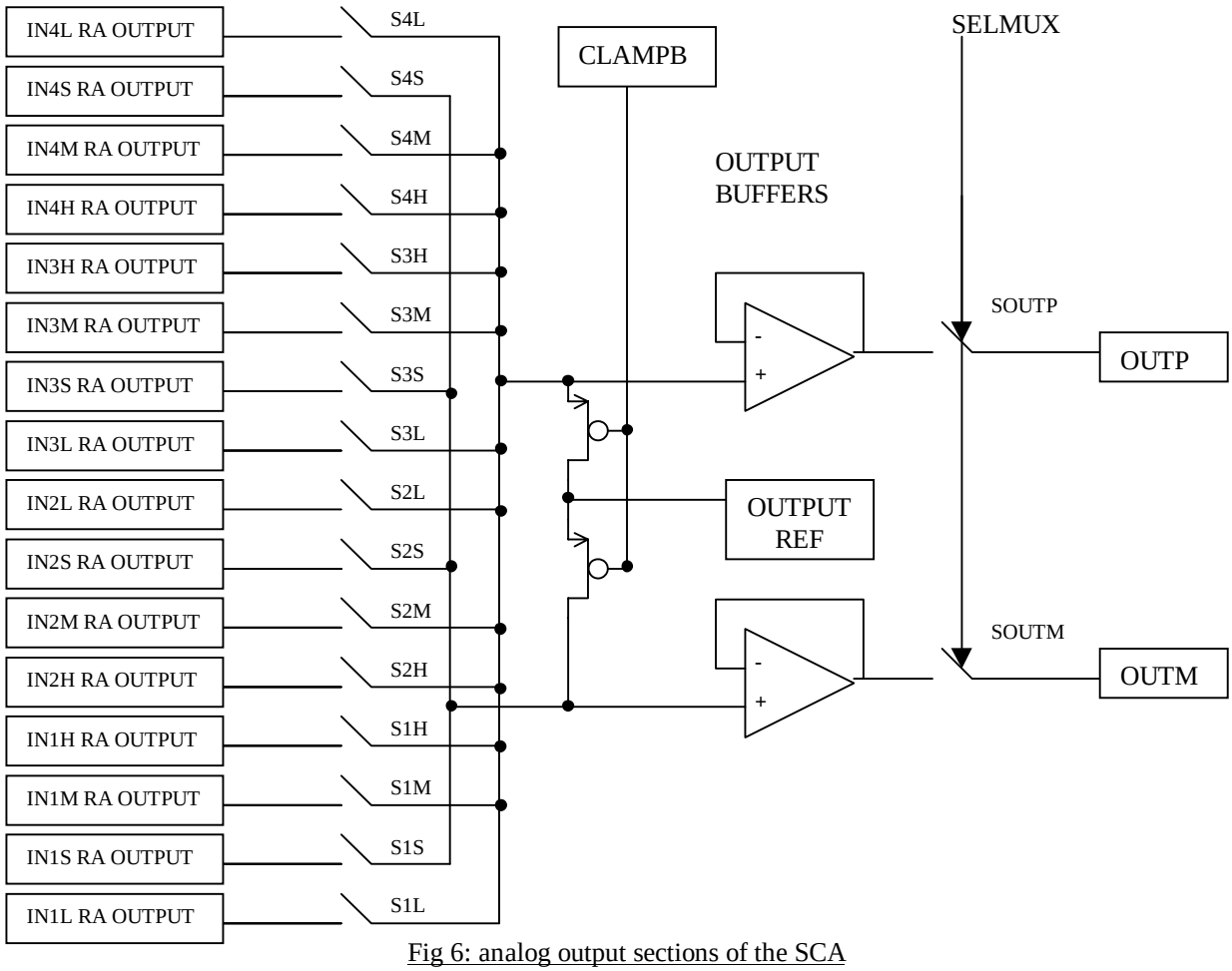


Fig 6: analog output sections of the SCA

The output buffers have the same structure than the write amplifiers (NMOS input). They are able to drive up to 30pF for 5Mhz read-out frequency and up to 20pF for 10Mhz read-out frequency. Their rms noise is 80uV rms when loaded by a 20pF capacitance.

As for the input buffer, the read-amplifiers bias currents is defined by an external resistor.
The static power consumption of each of the two buffers is 12.8mW including the bias branch.

To multiplex two SCAs towards the same ADC, the output buffers are insulated from the output pads by CMOS switches. The on resistance of these switches is 400 Ohm and varies of about 15% along the SCA voltage dynamic range. For this reason, and to keep good linearity performances, the electronics connected to the OUTP and OUTM pads needs to have a high input resistance (higher than 100 kOhm). That's the reason why voltage followers are implemented of the FEB in front of the subtractor. Moreover, the outputs of the SCA are never let in high Z state : the chip with parity zero is allways driving the line except if the other parity is being readout.

2.2.6 Noise and output signal filtering.

Eldo transient noise simulation gave results in good agreement with expression (1) and measurements. The total rms noise is evaluated to 260uV, and is dominated by the noise of the read amplifier (200uV rms). The input section noise (terms 1 and 2 in the (1) expression) is only 80uV rms. As the noise of the read amplifier is not sampled before digitization, it can be filtered before the ADC by a RC network (33 ohms and 270pF recommended).

2.3 Digital part.

The control logics is divided into two parts which are physically completely separated and which have their own power supplies. All the internal digital signals are CMOS signals with VSS low state and VDD high state. All the building blocks are full custom made. All the flip-flops and registers use gated-inverter based master-slave flip-flops.

2.3.1 Addressing scheme.

In order to reduce the digital to analog coupling the addresses generated by the controller corresponding to the 141 first cells of the SCA are encoded in Gray code. In this particular code, an increment of 1 always corresponds to the change of only one bit at a time.

The cells 141 to 143 (the first cell of a raw is zero) have their own code. With this code, the 141 to 142, 142 to 143, and 143 to 0 increments correspond also to only one bit changing.

One can notice that this addressing will be useful only if the cells are always addressed in the monotonic way. This is no more true when the pipeline is almost full, that is to say when the system is running close to the maximum trigger rate.

The write addresses are sent in parallel while the read addresses are sent serially at the read clock (RCK) rate.

2.3.2 Digital input buffers.

All the fast digital signals used for read as for write control are sent in differential low voltage (the two inputs are defined by the P and M suffixes). They are converted into CMOS levels by 'DIFF' blocks. The latter are composed by two CMOS comparators.

The one with the P phase connected to the positive input and the M phase connected to the negative output generates the positive CMOS signal. The other comparator, with the P phase connected to the negative input and the M phase connected to the positive output generates the inverted CMOS signal. This architecture, even if it doesn't offer the best power consumption efficiency, generates two perfectly complementary signals .

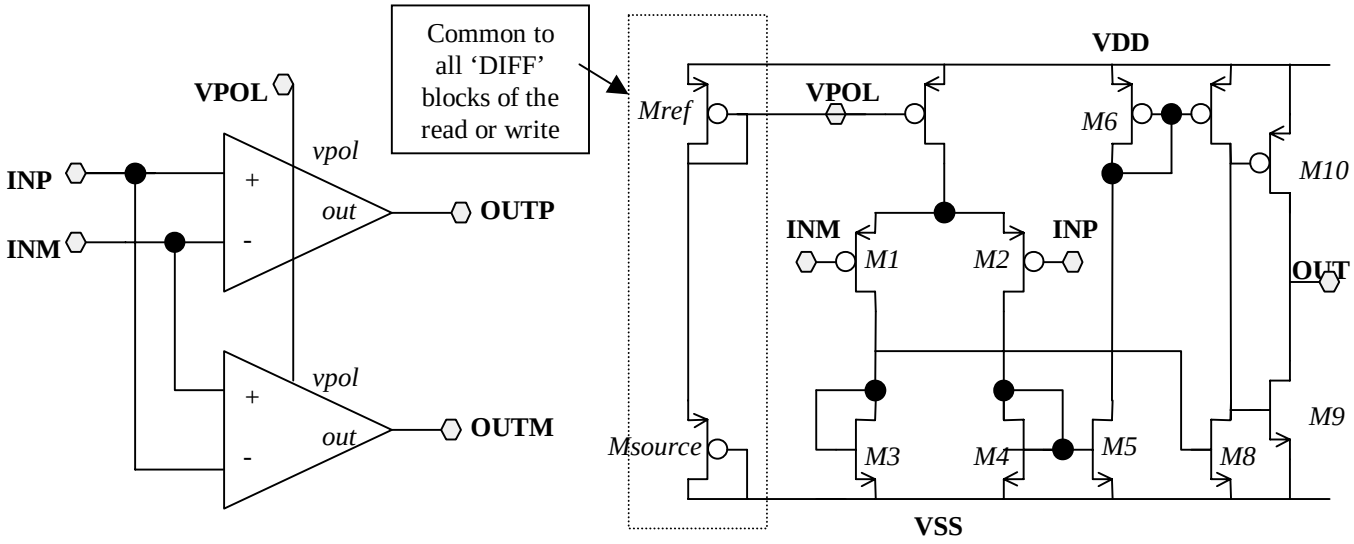


Fig 7: low voltage to CMOS 'DIFF'translators

The both comparators have PMOS inputs, so that the common mode voltage range acceptable for the input signal is between VSS and VDD - 1.2V, its minimum swing being 100mV. In the case of DC coupling (i.e. VSS=-1.7V, VDD=3.3V), the DIFF input stage is compatible with ECL, both end terminated PECL and LVDS differential signals.

The bias current of the DIFF blocks is internally set by a current reference composed by Msource-Mref. The gate potential of Mref (diode connected transistor) is bussed to the gate of all M0 transistors.

There are two independent pairs Msource-Mref in the circuit, one for the write commands and the other for the read commands. The gate voltages of the two MREFs transistors are respectively connected to RBIAS and WBIAS (through the connection "VPOL"on Fig 7). These two nodes have to be externally decoupled to VDD by a 100nF capacitor.

The DMILL circuit will also work if a resistor are connected between RBIAS and VSS or WBIAS and VSS as needed for the HP version of the chip. In this case the digital input buffer power consumption will be doubled.

2.3.3 Write control logics.

The functionalities of this block are to decode the write addresses and then to generate the write switch commands with the correct accurate timing.

The 8-bit address and the write clock (WCK) are sent to the chip in differential low voltage. They are immediately converted at the input of the chip into CMOS levels by 'DIFF' translators (see 2.2.2). Then, on the falling edge of the write clock, the write address is stored in the WA register.

The 8-bit output of this register is pre-decoded into 4 groups of four signals, 2 bits at a time, by an asynchronous AND gate based decoder. Inside each group, each of these 4 signals flags one of the four possible values of the two corresponding bits. The 16 (4 x 4) resulting lines are then bussed to 144 synchronous 4-input decoders such as the one of Fig 8.

When cp is low, the node n1 is set to 1. As cp (the write clock) rises to 1, the n1 node is set to 0 if the four inputs of the decoder are 1 ; else it stays at the 1 state. When cp2 goes to 1 this level is authorized to propagate, inverted, into the output node.

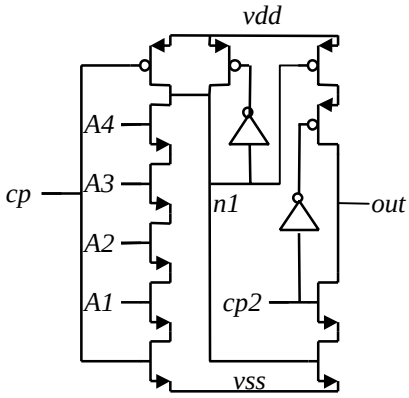


Fig 8: 4-input synchronous decoder

The resulting state is then stored on the output node parasitic capacitance until the next write clock cycle. Thus the timing of the write operation is only defined by the rising edge of cp2 (wck) and will not be address dependent..

At the output of the decoder the signal is buffered (RP<0:143>) to drive the gates of the NMOS write switches and also inverted then buffered with a delay of about 2ns on the rising edge. The resulting signals (RM<0:143>) drive the gates of the PMOS write switches. The sampling time, defined by the falling edge of the RP signal, is very accurate because only defined by cp2. The resulting typical delay between the rising edge of the differential low voltage input write clock (WCKP-WCKM) and the sampling time is 4ns.

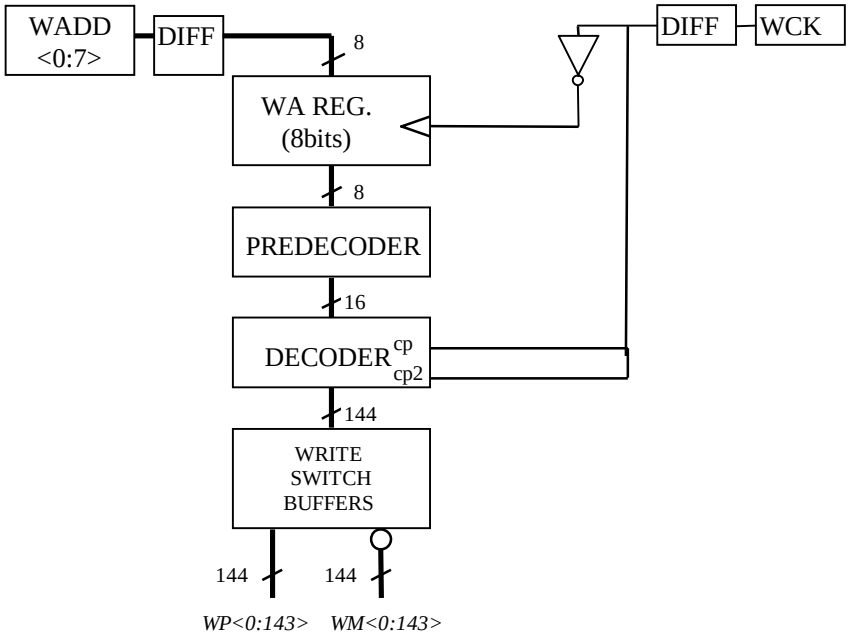


Fig 9: block diagram of the write control logics

2.3.4 Read-out control logics.

The read-out command block generates all the commands necessary for :

- the read-out of a capacitor : read-address decoding, reset and read signals sequencing.

- the internal multiplexing : generation and sequencing of the signals commanding the switches connected to the input of the output buffers.
- multiplexing between two chips towards a single ADC.

All the fast signals (RD, RDCK, SD, G0, G1) used to control the readout operation are provided in differential low voltage to the chip. These signals are translated into CMOS levels, immediately at the input of the chip, by the 'DIFF' bloc described in (2.3.2).

The mode bits (M, MUON) which are purely static signals are provided in CMOS levels.

If MUON=0, the circuit will operate in calorimeter mode. The twelve inputs have to correspond to four 3-gain channels. Thus the sequencing is optimized to read only one of the three gain by channel during each read cycle. In this mode, the circuit has been designed to run with a 200ns period read clock (RCK).

If MUON=1, then the circuit will operate in the *muon* mode which implies to multiplex sequentially the output of the twelve channels towards the ADC. In this mode, the circuit can run with a 125ns read clock (RCK).

The parity (M) bit is only used in the calorimeter mode. The address decoding and the read-out and multiplexing sequencing is delayed by four read-clock periods only if M=1. This allows interleaving towards a single ADC the data coming from another SCA with the opposed parity, thus sharing the same address and command lines. The SCA with the parity 0 is currently the standard one (not mirrored).

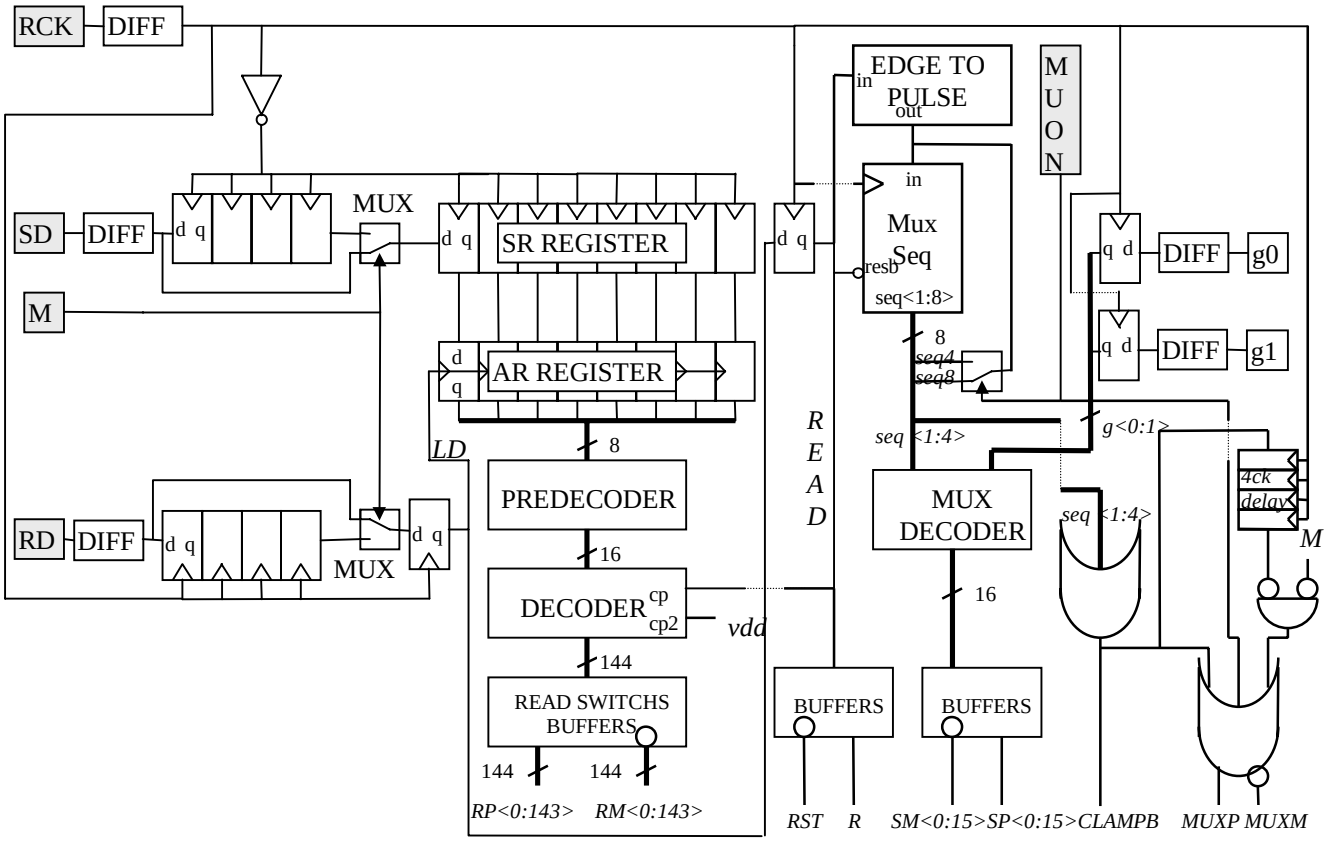


Fig 10: Block diagram of the readout control logics

For each sample, the 8-bit read address is sent serially (MSB first) from the controller to the chip over the SD signal at the read clock frequency (5 Mhz). If the parity bit (M) value is 1, the SD signal is delayed in a 4-bit shift register clocked by the negative edge of RCK. If the parity bit (M) value is 0, the SD signal is not delayed.

The resulting signal is pushed and shifted into a 8-bit shift-register (SR) also clocked by the negative edge of RCK. The read frame signal RD is the master of the read sequence. If the parity bit (M) value is 1, it is delayed in a 4-bit shift register clocked by the rising edge of RCK.

If the parity bit (M) value is 0, the RD signal is not delayed. The resulting signal is then resynchronized in a D flip-flop (dff) clocked by the rising edge of RCK. The output of this dff is the LD signal. This LD signal (synchronous with the rising edge of RCK) constitutes the command allowing to parallely load the 8-bit AR register with the contents of the SR register thus achieving the serial-to-parallel conversion of the read address.

Then, as for the write operation (see 2.2.3), the read-address is pre-decoded into 16 lines and finally decoded. As the timing issues are less critical than for write operation, the cp2 line of the decoder is connected to vdd. Thus the decoder is simply enabled by the READ signal connected to its cp input. The READ signal is the LD signal delayed by a dff clocked by the rising edge of RCK. This READ signal, buffered, constitutes the R signal, the same inverted being the RST signal. The both are used to perform the reset operation (see 2.2.4).

The 144 outputs of the decoder are buffered and inverted to form the two phases of the read-switches commands (RP<0:143>, RM<0:143>). As mentioned in 2.2.4, the phases of R, RST, RP and RM are carefully controlled.

The rising edge of the READ signal is converted into a positive pulse of one read clock period duration. This pulse enters the 8-phase multiplexer sequencer. The 2 gain inputs (g0 and g1) are synchronized by the rising edge of RCK. The two signals obtained ANDing the gains and the 4 first phases of the sequencer (seq<1:4>) are decoded then bufferised to generate the commands of the 16->2 output multiplexer (SM<0:15>,SP<0:15>).

In the case of MUON operation (MUON=1), the input of the sequencer is fed back by its 4th flip-flop. In the case of calorimeter operation (MUON=0), the input of the sequencer is fed back by its 8th flip-flop. In the both cases, the sequencer is reset when the falling edge of READ is detected.

The signal allowing the clamping (CLAMPB, negative logic) of the output multiplexer to the reference signal when the chip is not read is generated by the ‘or’ of the 4 first phases of the sequencer.

The two phases (MUXP,MUXM) used for the command of the switch connecting the two output buffers to the output pins are generated by the following logical combination :

MUXP = (CLAMPB + MUON + not (CLAMPB delayed by 4 RCK) . not (M))

So that :

- if MUON=1 the switches are always closed.

- in calorimeter mode (MUON=0):

- if M=1, the output switches are close only during the 4 first phases of the sequencer.
- if M=0, the output switches are always closed excepted during the 4 read clock period following the 4 first phases of the multiplexer sequence (i.e. when the sequencer of the chip with the opposite parity associated with the same ADC is in one of its 4 first phases).

The table 1 summarizes the order of the channel multiplexing depending on the value of the gain bits.

Phase # of the multiplexing	**G1**	**G0**	**Input corresponding to the Signal multiplexed to OUTP**	**Input corresponding to the Signal multiplexed to OUTM**
1	0	1	IN1L	IN1S
1	1	1	IN1M	IN1S
1	1	0	IN1H	IN1S
2	0	1	IN2L	IN2S
2	1	1	IN2M	IN2S
2	1	0	IN2H	IN2S
3	0	1	IN3L	IN3S
3	1	1	IN3M	IN3S
3	1	0	IN3H	IN3S
4	0	1	IN4L	IN4S
4	1	1	IN4M	IN4S
4	1	0	IN4H	IN4S

Table 1 : signal paths towards the analog outputs

Timing diagrams issued from Eldo simulations show the read sequence operation for different case of MUON and M values are given in appendix I.

3. PRACTICAL ASPECTS OF THE DESIGN

3.1 Design methodology.

The DMILL DDK V3.0 Design Kit has been used to check the design.
The design has been performed using the standard Cadence Analog Artist flow including :

- Simulations
- Layout
- Design Rules Checking
- Layout Versus Schematic Checking
- Parasitic Elements Extraction and post-layout simulation.

Concerning this last point :

- due to the special array geometry of the design where most of the parasitic capacitances are due to a sum of very small contributions (crossing between vertical and horizontal lines which can be ignored by the extractor), these types of parasitic elements have been extracted manually.
- No parasitic resistor extraction has been performed.
- No “back side” extraction has been performed.

3.2 Models and simulator used.

The HAMAC circuit has been originally designed using the spice lvl3 model parameters provided by TEMIC at the beginning of the process availability. The circuit has been mostly re-simulated using the BSIM V3.3 model, using more accurate parameters, provided by MHS in June 1998. This new set includes worst cases and post-irradiated parameters (10 Mrad). The key points of the circuit have been checked using these worst case parameters.

The simulators used are :

- SPECTRES (Cadence), used for analog simulation of basic blocks.
- ELDO (MENTOR), used in particular in OSR mode to simulate the digital blocks, for global simulations and for transient noise simulations.

These simulations have been performed including the parasitic elements (see 3.1). For more security, the read and write parts have also been successfully performed using read and write clocks with frequency at least double of the nominal ones (i.e. 10MHz for the read-clock and 100MHz for the write clock).

As it was impossible with the tools used (software + workstation) to simulate the whole design with simultaneous read and write, the global design has been simulated shared in two sections :

- write section : whole digital block + analog block including a 16*16 capacitor array + capacitance and parasitic elements of the rest of the array.
- read and output section : whole digital block + analog read and output block including a 16*16 capacitor array + capacitance and parasitic elements of the rest of the array.

3.3 Anti-ESD PROTECTIONS

All the pins (excepted OUTP and OUTM) are protected against positive or negative Electro-Static Discharges.

Special local power supplies lines (see pin-out section) are used to connect the protections to avoid capacitance couplings between signal and power supplies.

- the analog and digital inputs (excepted the signal inputs) are protected by standard OFF-MODE NMOS protections with surface reduced by a factor two with respect to DMILL Design KIT protections.

- the analog signal inputs are protected by similar protections but whose NMOS connected to VDD has its bulk connected to VSS. This type of input can accept transient signals up to VDD+2V without input impedance change (may be needed in case of AC coupling between the shaper and the SCA).

- all the power supply pins are protected :

* VDD to VSS by NMOS based protections (DMILL standard ones)
* VSS1 to VSS2 or VDD1 to VDD2 by diodes based protections (DMILL standard diodes).

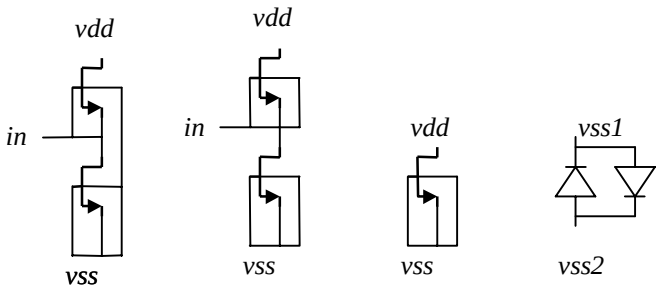


Fig 11: anti ESD protections

3.4 Guard rings.

To limit the digital to analog couplings, each block of the circuit is surrounded by guard rings individually connected to Kelvin points which are in fact special pin externally connected to the board ground. The two functions of these rings are :

- to screen couplings through the top silicon via trench parasitic lateral capacitors.
- to present a very low impedance in order to collect the charges injected into the back silicon.

Those rings are obtained by implanting a deep collector layer inside two trenches defined by a GENPMOS area.

3.5 Physical data.

The chip contains 45000 transistors, 2384 capacitors on a 4500um*4400um area.

4 PACKAGING, PINOUT AND RECOMMENDED CONNECTIONS OF THE CHIP .

The HAMAC chip is packaged into the same package used for the shaper. It is a 100 pin plastic rectangular QFP package with a 0.65mm pitch.

The body size of this package is 14mm*20mm. Its footprint is 17.2mm*23.2mm, its thickness is 2.7mm.

The leadframe used is the 100L 315*315 QFP from QPL LIMITED.

4.1 Standard chip.

PIN-OUT OF THE HAMAC CHIP (STANDARD VERSION) (1/2)

PIN	NAME	DESCRIPTION
1	VSS*	VSS CONNECTED TO THE LEADFRAME
2	M	PARITY BIT (Sometimes called PARITY elsewhere)
3	RCLKM	NEGATIVE PHASE OF THE READ CLOCK
4	RCLKP	POSITIVE PHASE OF THE READ CLOCK
5	SDM	NEGATIVE PHASE OF THE SERIAL READ ADDRESS
6	SDP	POSITIVE PHASE OF THE SERIAL READ ADDRESS
7	RDM	NEGATIVE PHASE OF THE READ FRAME
8	RDP	POSITIVE PHASE OF THE READ FRAME
9	MUON	MUON MODE SELECTOR (Sometimes called EX elsewhere)
10	VSSDR	VSS OF THE DIGITAL READ PART
11	VDDPR	VDD OF PROTECTIONS FOR DIGITAL READ PART
12	VDDDR	VDD OF THE DIGITAL READ PART
13	RBIAS	BIAS CONTROL OF THE DIGITAL INPUT BUFFERS FOR READ
14	VSSPR	VSS OF PROTECTIONS FOR DIGITAL READ PART
15	VSSPR	VSS OF PROTECTIONS FOR DIGITAL READ PART
16	VSSPR	VSS OF PROTECTIONS FOR DIGITAL READ PART
17	NC	NOT CONNECTED
18	VSSRG	VSS FOR GUARD RING
19	VSSRG	VSS FOR GUARD RING
20	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
21	VSSW	VSS FOR ANALOG WRITE PART
22	VSSW	VSS FOR ANALOG WRITE PART
23	VDDA2	VDD FOR ANALOG WRITE PART
24	VDDA2	VDD FOR ANALOG WRITE PART
25	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
26	VREF	REFERENCE VOLTAGE INPUT FOR RETURN ANALOG BUFFERS
27	VSS*	VSS CONNECTED TO THE LEAFRAME
28	BIASIN	BIAS CONTROL OF ANALOG INPUT BUFFERS
29	VCOM	REFERENCE VOLTAGE OUTPUT FOR RETURN ANALOG BUFFERS
30	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
31	IN4L	4th CHANNEL LOW GAIN INPUT
32	IN4S	4th CHANNEL SLAVE INPUT
33	IN4M	4th CHANNEL MEDIUM GAIN INPUT
34	IN4H	4th CHANNEL HIGH GAIN INPUT
35	GND	GROUND SHIELDING BETWEEN INPUTS
36	IN3H	3rd CHANNEL HIGH GAIN INPUT
37	IN3M	3rd CHANNEL MEDIUM GAIN INPUT
38	IN3S	3rd CHANNEL SLAVE INPUT
39	IN3L	3rd CHANNEL LOW GAIN INPUT
40	GND	GROUND SHIELDING BETWEEN INPUTS
41	IN2L	2nd CHANNEL LOW GAIN INPUT
42	IN2S	2nd CHANNEL SLAVE INPUT
43	IN2M	2nd CHANNEL MEDIUM GAIN INPUT
44	IN2H	2nd CHANNEL HIGH GAIN INPUT
45	GND	GROUND SHIELDING BETWEEN INPUTS
46	IN1H	1st CHANNEL HIGH GAIN INPUT
47	IN1M	1st CHANNEL MEDIUM GAIN INPUT
48	IN1S	1st CHANNEL SLAVE INPUT
49	IN1L	1st CHANNEL LOW GAIN INPUT
50	VSSGR	VSS FOR GUARD RING

PIN-OUT OF THE HAMAC CHIP (STANDARD VERSION) (2/2)

PIN	NAME	DESCRIPTION
51	VSSGR	VSS FOR GUARD RING
52	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
53	VSS*	VSS CONNECTED TO THE LEADFRAME
54	WCLKP	POSITIVE PHASE OF THE WRITE CLOCK
55	WCLKM	NEGATIVE PHASE OF THE WRITE CLOCK
56	NC	NOT CONNECTED
57	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
58	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
59	WA1P	POSITIVE PHASE OF THE WRITE ADDRESS BIT1
60	WA1M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT1
61	WA2P	POSITIVE PHASE OF THE WRITE ADDRESS BIT2
62	WA2M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT2
63	WA3P	POSITIVE PHASE OF THE WRITE ADDRESS BIT3
64	WA3M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT3
65	WA4P	POSITIVE PHASE OF THE WRITE ADDRESS BIT4
66	WA4M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT4
67	WA5P	POSITIVE PHASE OF THE WRITE ADDRESS BIT5
68	WA5M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT5
69	WA6P	POSITIVE PHASE OF THE WRITE ADDRESS BIT6
70	WA6M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT6
71	WA7P	POSITIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
72	WA7M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
73	VSSGR	VSS FOR GUARD RING
74	WBIAS	BIAS CONTROL OF THE DIGITAL INPUT BUFFERS FOR WRITE
75	NC	NOT CONNECTED
76	VSSDW	VSS FOR THE DIGITAL WRITE PART
77	VSS*	VSS CONNECTED TO THE LEAFRAME
78	VSSDW	VSS FOR THE DIGITAL WRITE PART
79	VDDDW	VDD FOR THEN DIGITAL WRITE PART
80	VDDDW2	VDD FOR THEN DIGITAL WRITE PART
81	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
82	PBIAS	BIAS CONTROL OF THE ANALOG READ AMPLIFIERS
83	VSSGR	VSS FOR GUARD RING
84	VSSPO	VSS OF PROTECTIONS FOR ANALOG OUTPUT PART
85	VCOMOUT	REFERENCE VOLTAGE FOR READ AMPLIFIERS AND OUTPUT
86	BBIAS	BIAS CONTROL OF THE ANALOG OUTPUT BUFFERS
87	OUTM	SLAVE ANALOG OUTPUT
88	OUTP	SIGNAL ANALOG OUTPUT
89	VSSPO	VSS OF PROTECTIONS FOR ANALOG OUTPUT PART
90	VSSO	VSS OF THE OUTPUT PART
91	VSSR	VSS FOR THE ANALOG READ PART
92	VSSR	VSS FOR THE ANALOG READ PART
93	VDDR	VDD FOR THE ANALOG READ PART
94	VDDR	VDD FOR THE ANALOG READ PART
95	VDDO	VDD FOR THE ANALOG OUTPUT PART
96	VDDPO	VDD FOR THE PROTECTIONS OF ANALOG READ & OUTPUT PARTS
97	GAIN0M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
98	GAIN0P	POSITIVE PHASE OF THE GAIN SELECTION BIT0
99	GAIN1M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
100	GAIN1P	POSITIVE PHASE OF THE GAIN SELECTION BIT1

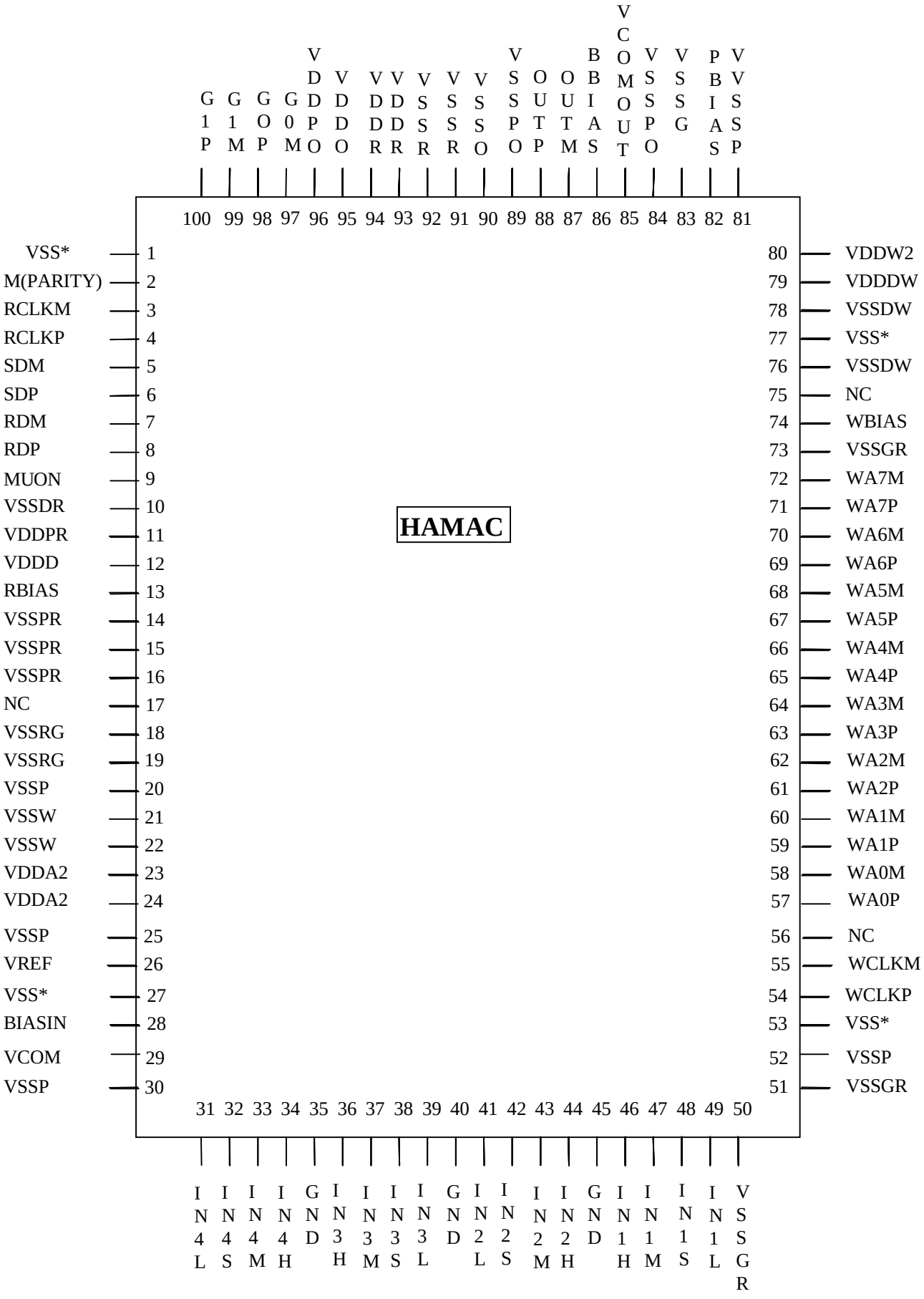
RECOMMENDED CABLING OF THE HAMAC CHIP (STANDARD VERSION) (1/2)

PIN	NAME	DESCRIPTION
1	VSS*	VSSA
2	M	VSSA or VSSD if M=0 else VDDA ou VDDD
3	RCLKM	NEGATIVE PHASE OF THE READ CLOCK
4	RCLKP	POSITIVE PHASE OF THE READ CLOCK
5	SDM	NEGATIVE PHASE OF THE SERIAL READ ADDRESS
6	SDP	POSITIVE PHASE OF THE SERIAL READ ADDRESS
7	RDM	NEGATIVE PHASE OF THE READ FRAME
8	RDP	POSITIVE PHASE OF THE READ FRAME
9	MUON	VSSA or VSSD if MUON=0 else VDDA ou VDDD (pulled down to vss internally)
10	VSSDR	VSSD
11	VDDPR	VDDD
12	VDDDR	VDDD
13	RBIAS	C=100nF to VDDD (also compatible with R=15.8K to VSSD)
14	VSSPR	VSSA
15	VSSPR	VSSA
16	VSSPR	VSSA
17	NC	VSSA
18	VSSRG	VSSA
19	VSSRG	VSSA
20	VSSP	VSSA
21	VSSW	VSSA
22	VSSW	VSSA
23	VDDA2	VDDA
24	VDDA2	VDDA
25	VSSP	VSSA
26	VREF	GNDA or remote GND of the shaper
27	VSS*	VSSA
28	BIASIN	R=2.4K to VDDA, C=100nF to VSSA
29	VCOM	C=1nF to GNDA
30	VSSP	VSSA
31	IN4L	4th CHANNEL LOW GAIN OUTPUT OF THE SHAPER
32	IN4S	REFERENCE OUTPUT OF THE SHAPER
33	IN4M	4th CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
34	IN4H	4th CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
35	GND	GNDA
36	IN3H	3rd CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
37	IN3M	3rd CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
38	IN3S	REFERENCE OUTPUT OF THE SHAPER
39	IN3L	3rd CHANNEL LOW GAIN OUTPUT OF THE SHAPER
40	GND	GNDA
41	IN2L	2nd CHANNEL LOW GAIN OUTPUT OF THE SHAPER
42	IN2S	REFERENCE OUTPUT OF THE SHAPER
43	IN2M	2nd CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
44	IN2H	2nd CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
45	GND	GNDA
46	IN1H	1st CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
47	IN1M	1st CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
48	IN1S	REFERENCE OUTPUT OF THE SHAPER
49	IN1L	1st CHANNEL LOW GAIN OUTPUT OF THE SHAPER
50	VSSGR	VSSA

RECOMMENDED CABLING OF THE HAMAC CHIP (STANDARD VERSION) (2/2)

PIN	NAME	DESCRIPTION
51	VSSGR	VSSA
52	VSSP	VSSA
53	VSS*	VSSA
54	WCLKP	POSITIVE PHASE OF THE WRITE CLOCK
55	WCLKM	NEGATIVE PHASE OF THE WRITE CLOCK
56	NC	VSSA
57	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
58	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
59	WA1P	POSITIVE PHASE OF THE WRITE ADDRESS BIT1
60	WA1M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT1
61	WA2P	POSITIVE PHASE OF THE WRITE ADDRESS BIT2
62	WA2M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT2
63	WA3P	POSITIVE PHASE OF THE WRITE ADDRESS BIT3
64	WA3M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT3
65	WA4P	POSITIVE PHASE OF THE WRITE ADDRESS BIT4
66	WA4M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT4
67	WA5P	POSITIVE PHASE OF THE WRITE ADDRESS BIT5
68	WA5M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT5
69	WA6P	POSITIVE PHASE OF THE WRITE ADDRESS BIT6
70	WA6M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT6
71	WA7P	POSITIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
72	WA7M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
73	VSSGR	VSSA
74	WBIAS	C=100nF to VDDD (also compatible with R=15.8K to VSSD)
75	NC	VSSA or VSSD
76	VSSDW	VSSD
77	VSS*	VSSA
78	VSSDW	VSSD
79	VDDDW	VDDD
80	VDDDW2	VDDD
81	VSSP	VSSA
82	PBIAS	R=2.7K to VSSA, 100nF to VDDA
83	VSSGR	VSSA
84	VSSPO	VSSA
85	VCOMOUT	GNDA
86	BBIAS	R=12.5K to VDDA, 100nF to VSSA
87	OUTM	SLAVE ANALOG OUTPUT TO HIGH IMPEDANCE NODE
88	OUTP	SIGNAL ANALOG OUTPUT TO HIGH IMPEDANCE NODE
89	VSSPO	VSSA
90	VSSO	VSSA
91	VSSR	VSSA
92	VSSR	VSSA
93	VDDR	VDDA
94	VDDR	VDDA
95	VDDO	VDDA
96	VDDPO	VDDA
97	GAIN0M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
98	GAIN0P	POSITIVE PHASE OF THE GAIN SELECTION BIT0
99	GAIN1M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
100	GAIN1P	POSITIVE PHASE OF THE GAIN SELECTION BIT1

HAMAC (STANDARD VERSION) PACKAGE



4.2 Mirrored chip.

PIN-OUT OF THE HAMAC CHIP (MIRRORED VERSION) (1/2)

PIN	NAME	DESCRIPTION
100	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
99	PBIAS	BIAS CONTROL OF THE ANALOG READ AMPLIFIERS
98	VSSGR	VSS FOR GUARD RING
97	VSSPO	VSS OF PROTECTIONS FOR ANALOG OUTPUT PART
96	VCOMOUT	REFERENCE VOLTAGE FOR READ AMPLIFIERS AND OUTPUT
95	BBIAS	BIAS CONTROL OF THE ANALOG OUTPUT BUFFERS
94	OUTM	SLAVE ANALOG OUTPUT
93	OUTP	SIGNAL ANALOG OUTPUT
92	VSSPO	VSS OF PROTECTIONS FOR ANALOG OUTPUT PART
91	VSSO	VSS OF THE OUTPUT PART
90	VSSR	VSS FOR THE ANALOG READ PART
89	VSSR	VSS FOR THE ANALOG READ PART
88	VDDR	VDD FOR THE ANALOG READ PART
87	VDDR	VDD FOR THE ANALOG READ PART
86	VDDO	VDD FOR THE ANALOG OUTPUT PART
85	VDDPO	VDD FOR THE PROTECTIONS OF ANALOG READ & OUTPUT PARTS
84	GAIN0M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
83	GAIN0P	POSITIVE PHASE OF THE GAIN SELECTION BIT0
82	GAIN1M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
81	GAIN1P	POSITIVE PHASE OF THE GAIN SELECTION BIT1
80	VSS*	VSS CONNECTED TO THE LEADFRAME
79	M	PARITY BIT (Sometimes called PARITY elsewhere)
78	RCLKM	NEGATIVE PHASE OF THE READ CLOCK
77	RCLKP	POSITIVE PHASE OF THE READ CLOCK
76	SDM	NEGATIVE PHASE OF THE SERIAL READ ADDRESS
75	SDP	POSITIVE PHASE OF THE SERIAL READ ADDRESS
74	RDM	NEGATIVE PHASE OF THE READ FRAME
73	RDP	POSITIVE PHASE OF THE READ FRAME
72	MUON	MUON MODE SELECTOR (Sometimes called EX elsewhere)
71	VSSDR	VSS OF THE DIGITAL READ PART
70	VDDPR	VDD OF PROTECTIONS FOR DIGITAL READ PART
69	VDDDR	VDD OF THE DIGITAL READ PART
68	RBIAS	BIAS CONTROL OF THE DIGITAL INPUT BUFFERS FOR READ
67	VSSPR	VSS OF PROTECTIONS FOR DIGITAL READ PART
66	VSSPR	VSS OF PROTECTIONS FOR DIGITAL READ PART
65	VSSPR	VSS OF PROTECTIONS FOR DIGITAL READ PART
64	NC	NOT CONNECTED
63	VSSRG	VSS FOR GUARD RING
62	VSSRG	VSS FOR GUARD RING
61	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
60	VSSW	VSS FOR ANALOG WRITE PART
59	VSSW	VSS FOR ANALOG WRITE PART
58	VDDA2	VDD FOR ANALOG WRITE PART
57	VDDA2	VDD FOR ANALOG WRITE PART
56	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
55	VREF	REFERENCE VOLTAGE INPUT FOR RETURN ANALOG BUFFERS
54	VSS*	VSS CONNECTED TO THE LEADFRAME
53	BIASIN	BIAS CONTROL OF ANALOG INPUT BUFFERS
52	VCOM	REFERENCE VOLTAGE OUTPUT FOR RETURN ANALOG BUFFERS
51	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART

PIN-OUT OF THE HAMAC CHIP (MIRRORED VERSION) (2/2)

PIN	NAME	DESCRIPTION
50	IN4L	4th CHANNEL LOW GAIN INPUT
49	IN4S	4th CHANNEL SLAVE INPUT
48	IN4M	4th CHANNEL MEDIUM GAIN INPUT
47	IN4H	4th CHANNEL HIGH GAIN INPUT
46	GND	GROUND SHIELDING BETWEEN INPUTS
45	IN3H	3rd CHANNEL HIGH GAIN INPUT
44	IN3M	3rd CHANNEL MEDIUM GAIN INPUT
43	IN3S	3rd CHANNEL SLAVE INPUT
42	IN3L	3rd CHANNEL LOW GAIN INPUT
41	GND	GROUND SHIELDING BETWEEN INPUTS
40	IN2L	2nd CHANNEL LOW GAIN INPUT
39	IN2S	2nd CHANNEL SLAVE INPUT
38	IN2M	2nd CHANNEL MEDIUM GAIN INPUT
37	IN2H	2nd CHANNEL HIGH GAIN INPUT
36	GND	GROUND SHIELDING BETWEEN INPUTS
35	IN1H	1st CHANNEL HIGH GAIN INPUT
34	IN1M	1st CHANNEL MEDIUM GAIN INPUT
33	IN1S	1st CHANNEL SLAVE INPUT
32	IN1L	1st CHANNEL LOW GAIN INPUT
31	VSSGR	VSS FOR GUARD RING
30	VSSGR	VSS FOR GUARD RING
29	VSSP	VSS OF PROTECTIONS FOR ANALOG WRITE PART
28	VSS*	VSS CONNECTED TO THE LEAFRAME
27	WCLKP	POSITIVE PHASE OF THE WRITE CLOCK
26	WCLKM	NEGATIVE PHASE OF THE WRITE CLOCK
25	NC	NOT CONNECTED
24	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
23	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
22	WA1P	POSITIVE PHASE OF THE WRITE ADDRESS BIT1
21	WA1M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT1
20	WA2P	POSITIVE PHASE OF THE WRITE ADDRESS BIT2
19	WA2M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT2
18	WA3P	POSITIVE PHASE OF THE WRITE ADDRESS BIT3
17	WA3M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT3
16	WA4P	POSITIVE PHASE OF THE WRITE ADDRESS BIT4
15	WA4M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT4
14	WA5P	POSITIVE PHASE OF THE WRITE ADDRESS BIT5
13	WA5M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT5
12	WA6P	POSITIVE PHASE OF THE WRITE ADDRESS BIT6
11	WA6M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT6
10	WA7P	POSITIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
9	WA7M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
8	VSSGR	VSS FOR GUARD RING
7	WBIAS	BIAS CONTROL OF THE DIGITAL INPUT BUFFERS FOR WRITE
6	NC	NOT CONNECTED
5	VSSDW	VSS FOR THE DIGITAL WRITE PART
4	VSS*	VSS CONNECTED TO THE LEAFRAME
3	VSSDW	VSS FOR THE DIGITAL WRITE PART
2	VDDDW	VDD FOR THEN DIGITAL WRITE PART
1	VDDDW2	VDD FOR THEN DIGITAL WRITE PART

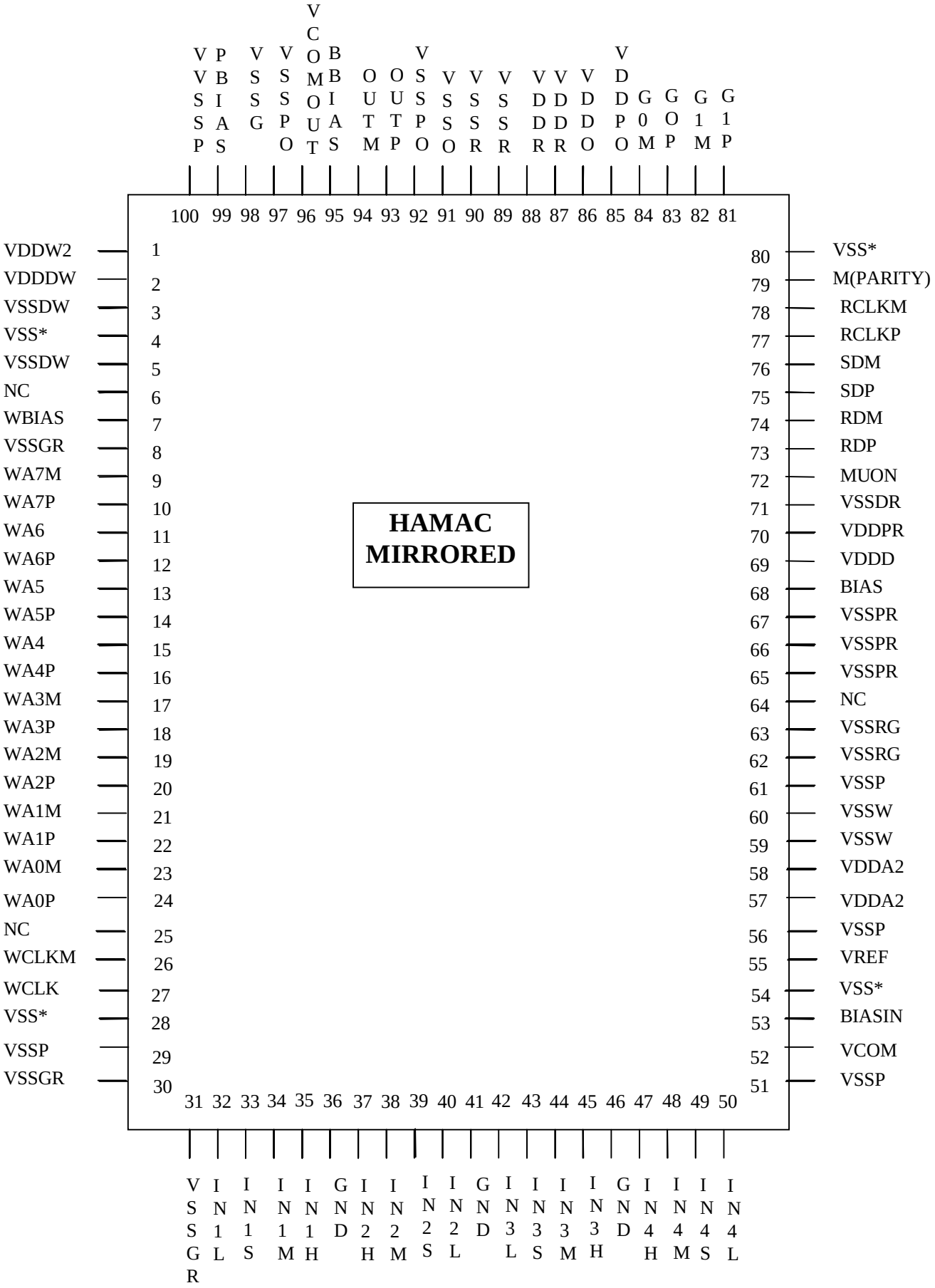
RECOMMENDED CABLING OF THE HAMAC CHIP (MIRRORED VERSION) (1/2)

PIN	NAME	DESCRIPTION
100	VSSP	VSSA
99	PBIAS	R=2.7K to VSSA, 100nF to VDDA
98	VSSGR	VSSA
97	VSSPO	VSSA
96	VCOMOUT	GNDA
95	BBIAS	R=12.5K to VDDA, 100nF to VSSA
94	OUTM	SLAVE ANALOG OUTPUT
93	OUTP	SIGNAL ANALOG OUTPUT
92	VSSPO	VSSA
91	VSSO	VSSA
90	VSSR	VSSA
89	VSSR	VSSA
88	VDDR	VDDA
87	VDDR	VDDA
86	VDDO	VDDA
85	VDDPO	VDDA
84	GAIN0M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
83	GAIN0P	POSITIVE PHASE OF THE GAIN SELECTION BIT0
82	GAIN1M	NEGATIVE PHASE OF THE GAIN SELECTION BIT0
81	GAIN1P	POSITIVE PHASE OF THE GAIN SELECTION BIT1
80	VSS*	VSSA
79	M	VSSA or VSSD if M=0 else VDDA or VDDD
78	RCLKM	NEGATIVE PHASE OF THE READ CLOCK
77	RCLKP	POSITIVE PHASE OF THE READ CLOCK
76	SDM	NEGATIVE PHASE OF THE SERIAL READ ADDRESS
75	SDP	POSITIVE PHASE OF THE SERIAL READ ADDRESS
74	RDM	NEGATIVE PHASE OF THE READ FRAME
73	RDP	POSITIVE PHASE OF THE READ FRAME
72	MUON	VSSA or VSSD if MUON=0 else VDDA or VDDD (pulled down to vss internally)
71	VSSDR	VSSD
70	VDDPR	VDDD
69	VDDDR	VDDD
68	RBIAS	C=100nF to VDDD (also compatible with R=15.8K to VSSD)
67	VSSPR	VSSA
66	VSSPR	VSSA
65	VSSPR	VSSA
64	NC	VSSA
63	VSSRG	VSSA
62	VSSRG	VSSA
61	VSSP	VSSA
60	VSSW	VSSA
59	VSSW	VSSA
58	VDDA2	VDDA
57	VDDA2	VDDA
56	VSSP	VSSA
55	VREF	GNDA or remote GND of the shaper
54	VSS*	VSSA
53	BIASIN	R=2.4K to VDDA, C=100nF to VSSA
52	VCOM	C=1nF to GNDA
51	VSSP	VSSA

RECOMMENDED CABLING OF THE HAMAC CHIP (MIRRORED VERSION) (2/2)

PIN	NAME	DESCRIPTION
50	IN4L	4th CHANNEL LOW GAIN OUTPUT OF THE SHAPER
49	IN4S	REFERENCE OUTPUT OF THE SHAPER
48	IN4M	4th CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
47	IN4H	4th CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
46	GND	GNDA
45	IN3H	3rd CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
44	IN3M	3rd CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
43	IN3S	REFERENCE OUTPUT OF THE SHAPER
42	IN3L	3rd CHANNEL LOW GAIN OUTPUT OF THE SHAPER
41	GND	GNDA
40	IN2L	2nd CHANNEL LOW GAIN OUTPUT OF THE SHAPER
39	IN2S	REFERENCE OUTPUT OF THE SHAPER
38	IN2M	2nd CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
37	IN2H	2nd CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
36	GND	GNDA
35	IN1H	1st CHANNEL HIGH GAIN OUTPUT OF THE SHAPER
34	IN1M	1st CHANNEL MEDIUM GAIN OUTPUT OF THE SHAPER
33	IN1S	REFERENCE OUTPUT OF THE SHAPER
32	IN1L	1st CHANNEL LOW GAIN OUTPUT OF THE SHAPER
31	VSSGR	VSSA
30	VSSGR	VSSA
29	VSSP	VSSA
28	VSS*	VSSA
27	WCLKP	POSITIVE PHASE OF THE WRITE CLOCK
26	WCLKM	NEGATIVE PHASE OF THE WRITE CLOCK
25	NC	VSSA
24	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
23	WA0P	POSITIVE PHASE OF THE WRITE ADDRESS BIT0 (LSB)
22	WA1P	POSITIVE PHASE OF THE WRITE ADDRESS BIT1
21	WA1M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT1
20	WA2P	POSITIVE PHASE OF THE WRITE ADDRESS BIT2
19	WA2M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT2
18	WA3P	POSITIVE PHASE OF THE WRITE ADDRESS BIT3
17	WA3M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT3
16	WA4P	POSITIVE PHASE OF THE WRITE ADDRESS BIT4
15	WA4M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT4
14	WA5P	POSITIVE PHASE OF THE WRITE ADDRESS BIT5
13	WA5M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT5
12	WA6P	POSITIVE PHASE OF THE WRITE ADDRESS BIT6
11	WA6M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT6
10	WA7P	POSITIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
9	WA7M	NEGATIVE PHASE OF THE WRITE ADDRESS BIT7 (MSB)
8	VSSGR	VSSA
7	WBIAS	C=100nF to VDDD (also compatible with R=15.8K to VSSD)
6	NC	VSSA or VSSD
5	VSSDW	VSSD
4	VSS*	VSSA
3	VSSDW	VSSD
2	VDDDW	VDDD
1	VDDDW2	VDDD

HAMAC (MIRRORED VERSION) PACKAGE



5 PRELIMINARY DATA SHEET and PSRR simulations.

5.1 PRELIMINARY DATA SHEET

This preliminary data sheet contains requirements and performances of the HAMAC chip. Most of them come from **simulation data**. Measurement results are described in section 7. The timings described here ensure a correct functionality of the circuit with DC coupling between shaper and the SCA.

NAME	Description	Min	Typ	Max	Unit
VDDA	ANALOG Positive power supply voltage		3.3		V
VSSA	ANALOG Negative power supply voltage		-1.7		V
VDDD	DIGITAL Positive power supply voltage		3.3		V
VSSD	DIGITAL Negative power supply voltage		-1.7		V
PWRD	DIGITAL Power Consumption		55		mW
PWRA	ANALOG Power Consumption		235		mW
Fw	WRITE CLOCK FREQUENCY		40		MHz
Frcalo	READ-OUT CLOCK FREQUENCY		5	8(muon)	MHz
dtwck	Write clock duty cycle	35	50	65	%
dtrck	Read clock duty cycle	30	50	70	%
twawckb	Time between end of write address change and falling edge of write clock	3			ns
twcks	Delay between rising edge of write clock and sampling	2	4	6	ns
tsdrckb	Time between SD and falling edge of read clock	3			ns
trdck	Time between RD and rising edge of read clock	3			ns
VCH	High level for ‘CMOS’ inputs	+1.3		3.3	V
VCL	Low level for ‘CMOS’ inputs	-1.7		+0.3	V
VLVH	Low voltage inputs High Level	-1.6		3.3	V
VLVL	Low voltage inputs Low Level	-1.7		2.1	V
VLVSW	Swing for Low voltage inputs	0.100	0.400	5	V
Cin	Input Pin capacitance		3		pF
Rin	Input Pin resistance	10M			Ohm
Cout	Analog Output capacitance		4		pF
Rout	Analog Output output resistance		400		Ohm
Zload	Minimum output load	100k			Ohm
BWi	Input Bandwidth		55		Mhz
tTRACK	TRACKING PHASE DURATION		23		ns
τRESET	DURATION OF THE RESET (BEFORE READ PHASE)		100		ns
τRA	Read amplifier time constant (read mode)	15			ns
τBUF	OUTPUT BUFFER TIME constant (30pF load)	8			ns

5.2 Power suplies rejection rejection.

The rejection of the SCA input section to spurious signals on the power supply voltages has been studied in simulation. These simulations include the write buffers and return bus buffer with their biasing and decoupling elements, the 144 capacitor cells and all the parasitic capacitive elements taking also into account the capacitors to the back silicon which is supposed to be connected to vss.

The rejections of the voltage across the storage capacitor to ac spurious signal on vss and vdd are plotted on fig 12.a and 12.b in four cases :

- single ended operation : the slave channel is not subtracted to the signal channel.
- differential operation (slave channel used) assuming a 5% mismatch of the bias current of the amplifiers of the signal and slave channel.
- differential operation (slave channel used) assuming a 0.1µm mismatch of the write switches gate length of the signal and slave cells.
- The last case is the rejection of the return voltage follower (see Figure 5).

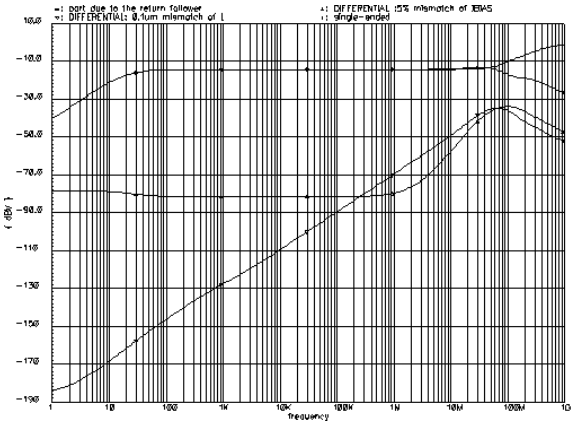


Fig 12a : PSRR to vss (current design)

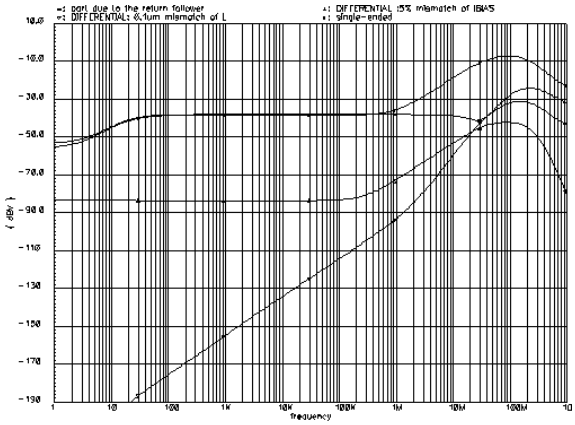


Fig 12b : PSRR to vdd (current design)

The PSSR to vss is low for intermediate frequencies in case of single ended operation. This is mainly due to the poor PSSR of the NMOS source follower used to bufferize the return bus.
For the same range of frequencies, the PSSR to vdd is 20dB better, but limited again by the return buffer one.
For frequencies above 1 MHz, the PSRR to the both power supplies starts to decrease. This is mainly due to the effect of parasitic capacitances between the switches command lines (connected to vss and vdd via CMOS inverters) and the write top and return busses. This effect is magnified by the fact that the write amplifier output impedance start to increase at these frequencies.

The PSSR to vss and vdd are dramatically improved by the use of the slave channel, even if some mismatches exist between the signal and the slave channel. Anyway, as the vss power supply is common to both the analog and the digital part of the chip, the poor PSSR to vss in single ended operation is a week point of the SCA chip which can be easily improved.

In the present circuit, the poor PSSR of the return bus follower is mainly due to the bulk connection of the Mfi NMOS transistors (see Figure 5) to vss. In the DMILL technology, each transistor can have its own separate substrate. In particular, it is allowed to connect the substrates of the Mfi and MFd NMOS transistors of fFigure 5 to their sources.
The PSSR to vdd could also be improved by increasing the gate length of th Mfi transistors. But it would result in an increase of the power consumption to keep these transistors transconductance constant.

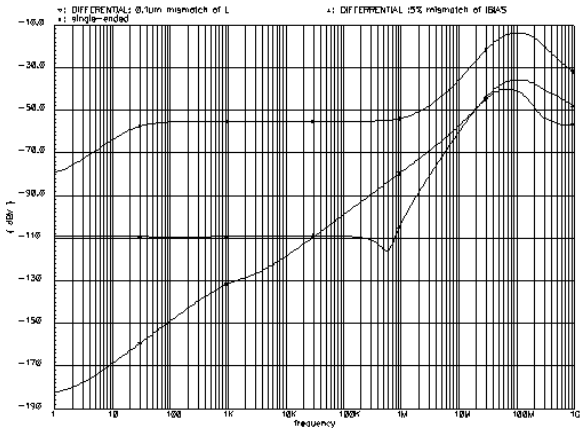


Fig 12c : PSRR to vss (improved design)

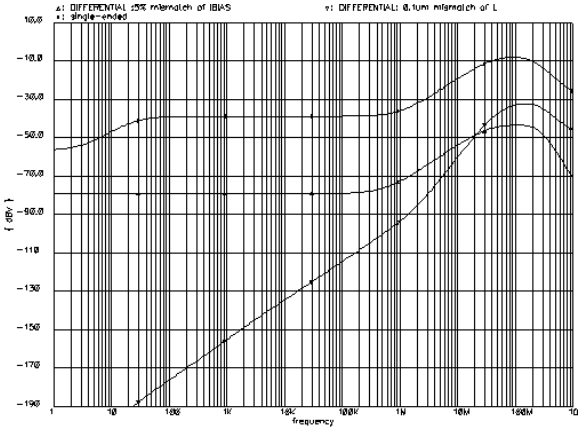


Fig 12d : PSRR to vdd (improved design)

The simulated PSSR to vss and vdd with the new substrate connection of the Mfi and MFd source followers are plotted on fig 12.c and 12.d. The increases of the PSSR to vss at low frequency is increased by 30 dB. The PSSR to vdd is unchanged. As it is easily achievable in the layout with any area penalty, this modification is highly desirable for the pre-production prototype (see section 9).

6 TEST BENCH SETUP.

6.1 Test setup in lab.

A specific test bench has been designed for testing the SCAs. It has to simulate the real working environment of the chips while allowing the most various measurements. It is based on a set of two boards, one VME "SPACMaster" board and one test board. The first one is master of the 10Mbit/s SPAC serial link [9] which drives the latter. This type of set-up allows to isolate completely the test board from any VME source of pickup, especially with the SPAC bus which is mute when not used.

A special care has been taken in the design of the test board to avoid couplings between analog and digital parts. It's obvious that in such a test bench, the quality of measurement awaited draws to strong choices as double global ground planes and differential digital signals.

The block diagram of the test board is shown in Fig 13a.

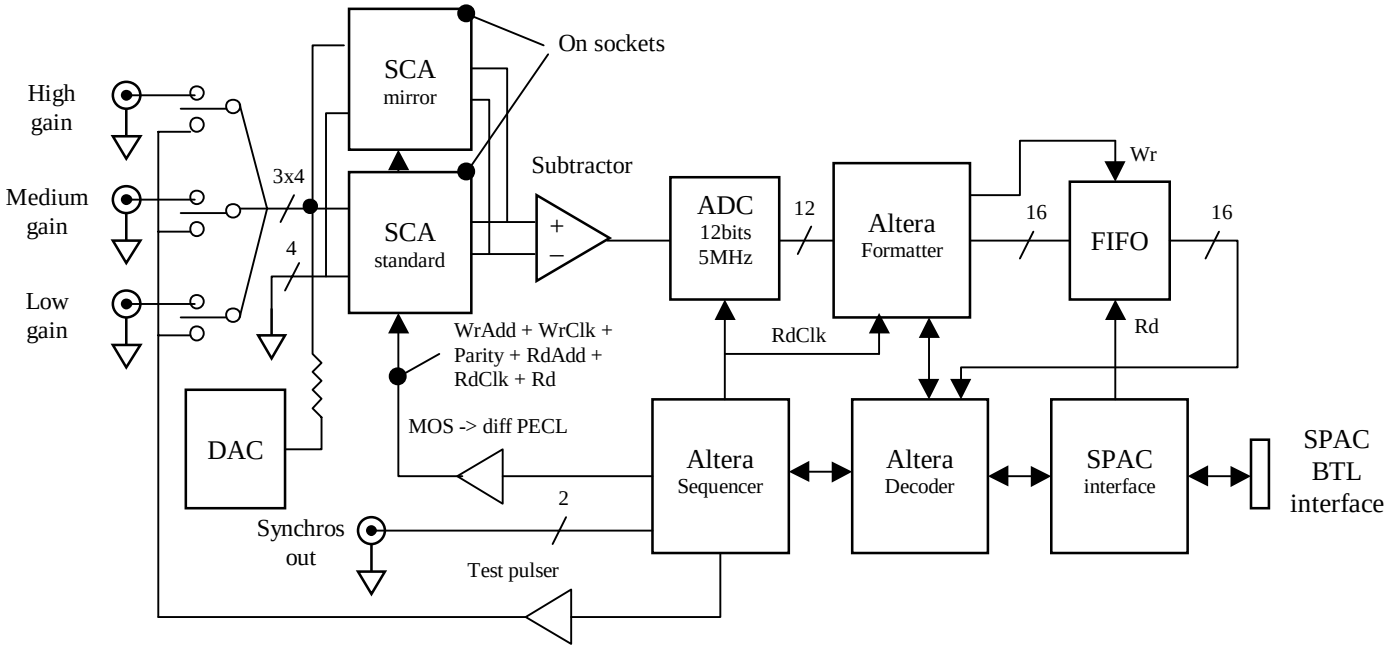


Fig 13a : Block diagram of the SCA test board

There is no standard SCA sequencer on this board. It is replaced by a custom very simplified system which however allows simultaneous write and read operations but also complex measurements. The test board is connected to a VME calibration board which sends a standard pulse to a preamp + shaper chain located just in front of the board input. Thus this bench allows a lot of different facilities :

- noise measurements which include white noise and fixed pattern noise
- calibration ramps (DC and transient)
- distributed sampling time skew measurement
- mean or single shot triggering.

A dedicated software has been developed on a Macintosh. It offers a totally graphical user interface (see Fig13b) and will be soon upgraded for the robotized test setup in sight of the production validation.

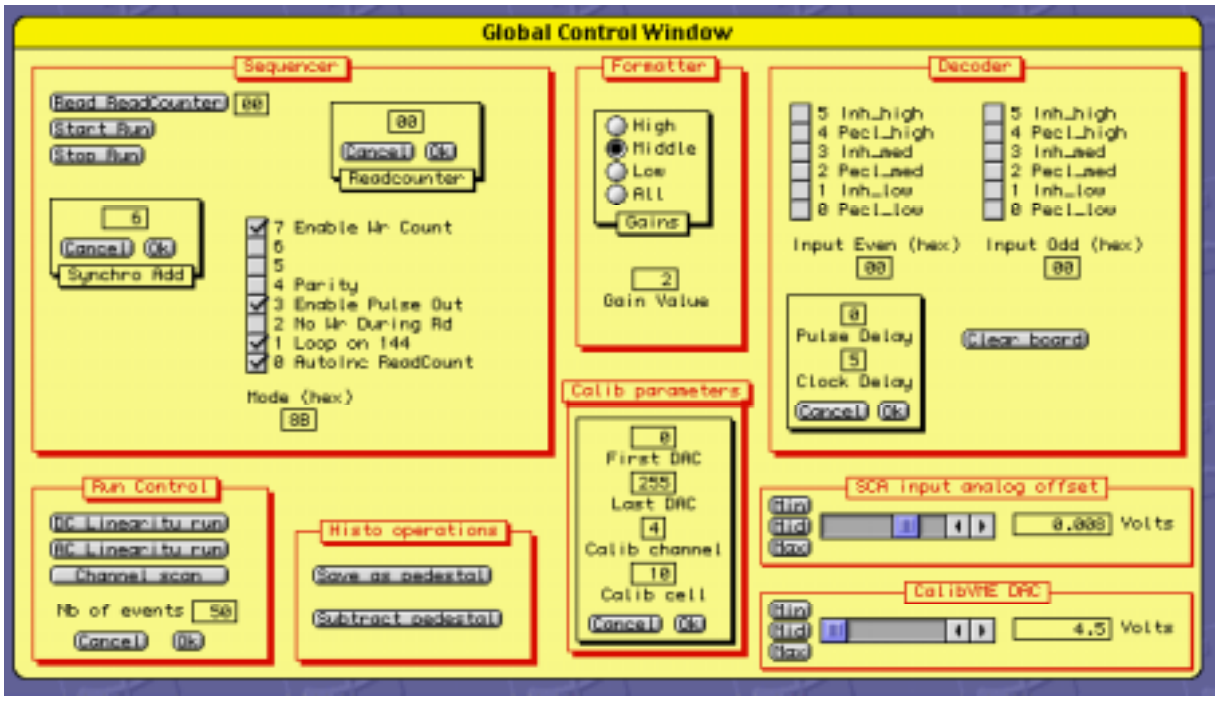


Fig 13b : interactive window of the test bench software

Both versions of the DMILL SCA have been tested on the bench. Those tests can be performed either with only one of the two versions mounted or with the both at the same time.

The main results obtained on the tested chips are presented below.

6.2 Test setup for production

A new test setup will be developed for the test of the production SCAs. It will be based on the use of a robot for manipulating the chips. The robot will be driven by a PC running under LabViews and connected with the Macintosh through a control register sited on the test board.

The main measurements for validating a chip will be the following :

- Fixed Pattern Noise : absolute limit for individual capacitors and for the mean value
- Total noise : idem

Those measurements will be performed over two different DC values :

- Pedestal level
- “High” DC level

A powerful test consisting in a scan of all the individual cells with individual pulses will also be performed to check the complete functionality of the circuit.

The channel pedestal dispersion will be measured and computed to verify the output multiplexor. A threshold will be set on this distribution.

The power consumption of all the supplies will also be monitored.

7 MEASUREMENT RESULTS

The measurements described here have been realized on the test bench described in 6. In this bench the SCAs are mounted on sockets. For this reason, the performances of the chip are probably slightly degraded. The measurements have been performed on DMILL V1.1, V1.2 and V2 chips and, for reference, on HP module 0 un-mirrored chip.

All the measurements have been performed in the calorimeter mode with a 40 MHz write clock and a 5 MHz read clock.

7.1 Statistics and Yield.

The following table summarizes the results of the tests performed at the reception of the DMILL chips:

BATCH/WAFER IDENTIFICATION	V1.1	V1.2	V2 wafer12	V2 wafer4	V2 wafer4 mirrored
NUMBER OF TESTED CHIPS	30	30	20	48	49
NUMBER OF GOOD CHIP	27	24	10	39	43
CHIP WITH 1or 2 bad cell	2	4	8	6	4
Other Problem	1	2	2	3	2
'Yield'	90%	80%	50%	81%	87%

All the chips come from batches with well centered main parameters excepted for the wafer 4 of batch V2. In this wafer, the RM1P+ parameter (resistance of contact between metal1 and P+ diffusion) is 10% higher than the maximum specified value.

An abnormal density of particular defects has been measured on the wafer 12 of batch V2. According to TEMIC experts, it can explain the poorer yield obtained on this wafer. In production, such a wafer would be rejected, because out of specifications.

Most of the bad chips have only one or two bad cells (the power consumption is normal for these chips). It implies that during the production test, it will be necessary to test all the memory cells of the SCA.

The yields are only indicative because of the lack of statistic. The wafer 4 of batch V2 gives a little more information. Indeed all the chips of these wafer were tested.

7.2 Power consumption.

The total power consumption measured on both V1.1, V1.2 and V2 chips is 290mW +/-5%. Almost the same power consumption is measured on HP chips.

7.3 DC range.

Fig 14.a and 14.b show typical DC linearity curve for the DMILL V1.1 and HP chip.

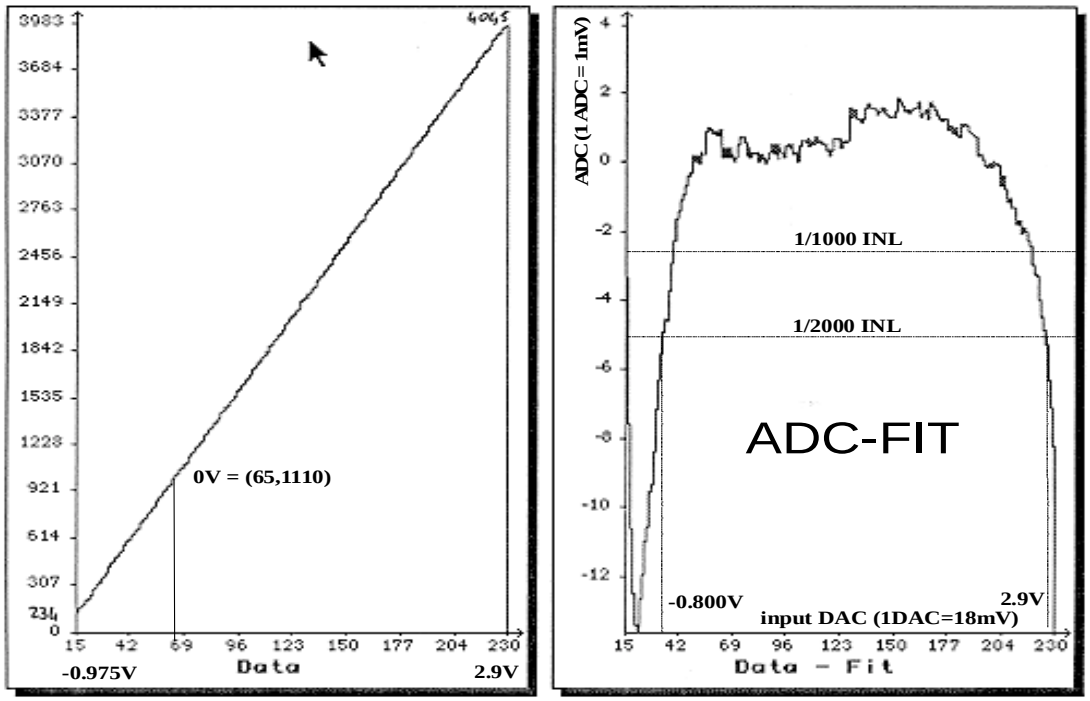


Fig 14.a : DC linearity of the DMILL chip (V1.1)

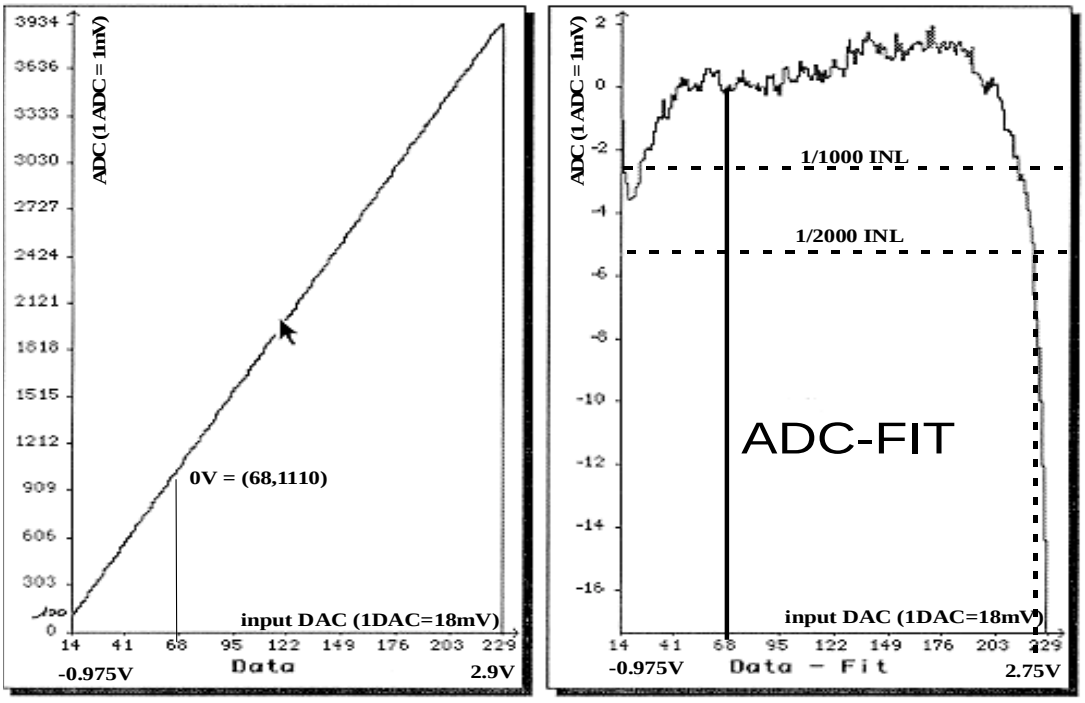


Fig 14.b : DC linearity plot of the HP chip

The results obtained for the DMILL chips coming from the V1.1, V1.2 and V2 batches are identical

From these plots are extracted :

- the input DC range with integral non linearity < 2/1000 defined as (data-fit)/2.5V.
  DMILL : -0.8V/2.9V. ***HP : -0.95V/2.75V***

- the DC gain (DCG) of the chips.
  DMILL : 0.995 ***HP : 0.990***

7.4 Noise and Fixed Sequence Noise.

The noise and the fixed sequence noise of the chips have been studied in simultaneous read and write operations. The chip was always addressed in the same order simulating low trigger rate condition. For these measurements, a gain of x11 was inserted between the SCA and the ADC input, so that 1 ADC count = 90uV.

The fig 15.a and 15.b show for both DMILL and HP chips :
- the total distribution of the baseline value. This distribution is called overall pedestal distribution and its rms value is called overall pedestal noise.
- the value of the mean baseline (pedestal) as a function of cell number. The rms value of the distribution of this last quantity is called fixed pattern noise or fixed sequence noise.
- the value of the rms noise as a function of cell number. The mean value of this distribution is called rms noise on pedestal.

The following table sums up the values measured for the various noise parameters for the different version of the chips. These values are the mean values obtained over each population.

	DMILL V1.1	**DMILL V1.2**	**DMILL V2w12**	**DMILL V2w4**	**DMILL V2W4M**	**HP**
Rms Noise (on pedestal) value (µV rms):	300	300	290	290	290	270
Rm pedestal dispersion Value (µV rms):	190	230	225	250	245	120
Sigma of Overall pedestal Distribution (µV rms)	360	375	365	375	375	300
DC dynamic range	13.3 bits	13.2 bits	13.2bits	13.2bits	13.2bits	**13.6bits**

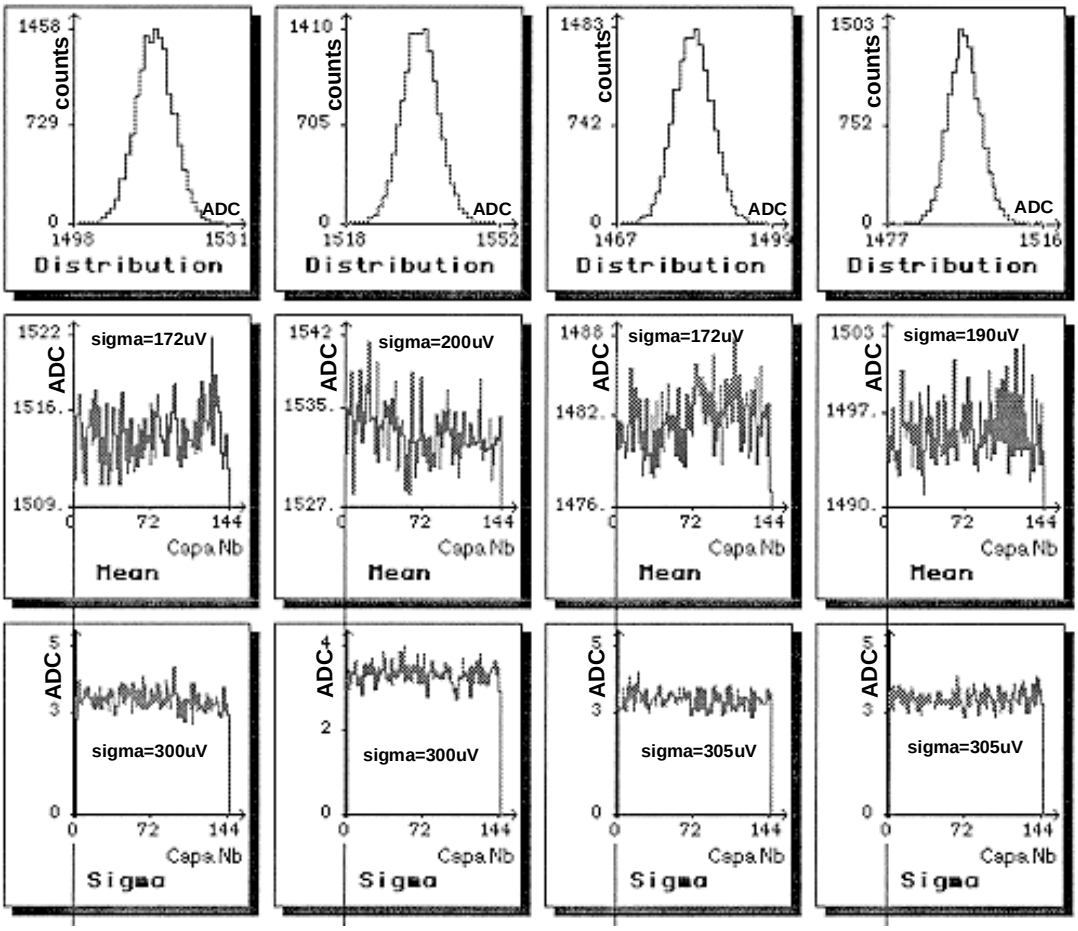
The performances of the HP chip are better than the DMILL ones, especially for the fixed pattern noise. As one major source of the fixed pattern is the mismatch from cell to cell of the charge injected by the S2 NMOS switch during the sampling, the highest DMILL value could be explained by the special NMOS structure in this technology. Indeed, in DMILL the NMOS width is defined by the N+ diffusion instead of the opening of the LOCOS as in standard technology.

But, even in DMILL, the rms value of the pedestal fixed sequence noise remains small. So that, it will not be necessary to perform a cell by cell compensation of this effect.

Figure 15.c shows a correlation plot for the pedestal of two channels in two cases. In the first case, the two channels, which correspond to two gains of the same calorimeter channel, share the same SCA slave channel, so that a part of their fixed pattern noise is correlated. In the second case, the two channels correspond to the same gain of two different calorimeter cells. In this case, there is no obvious visible structure coherent from channel to channel. An accurate evaluation of this correlation can be done only on a FEB equipped with a large number of SCA channels

The wafer backside metallization does not seem to improve the fixed pattern noise or the noise characteristics. So this operation does not seem to be useful for our application.

There is no visible difference of noise an fixed pattern between the chips of batch V2 wafer 4 packaged in a standard way and the ones packaged upside down.

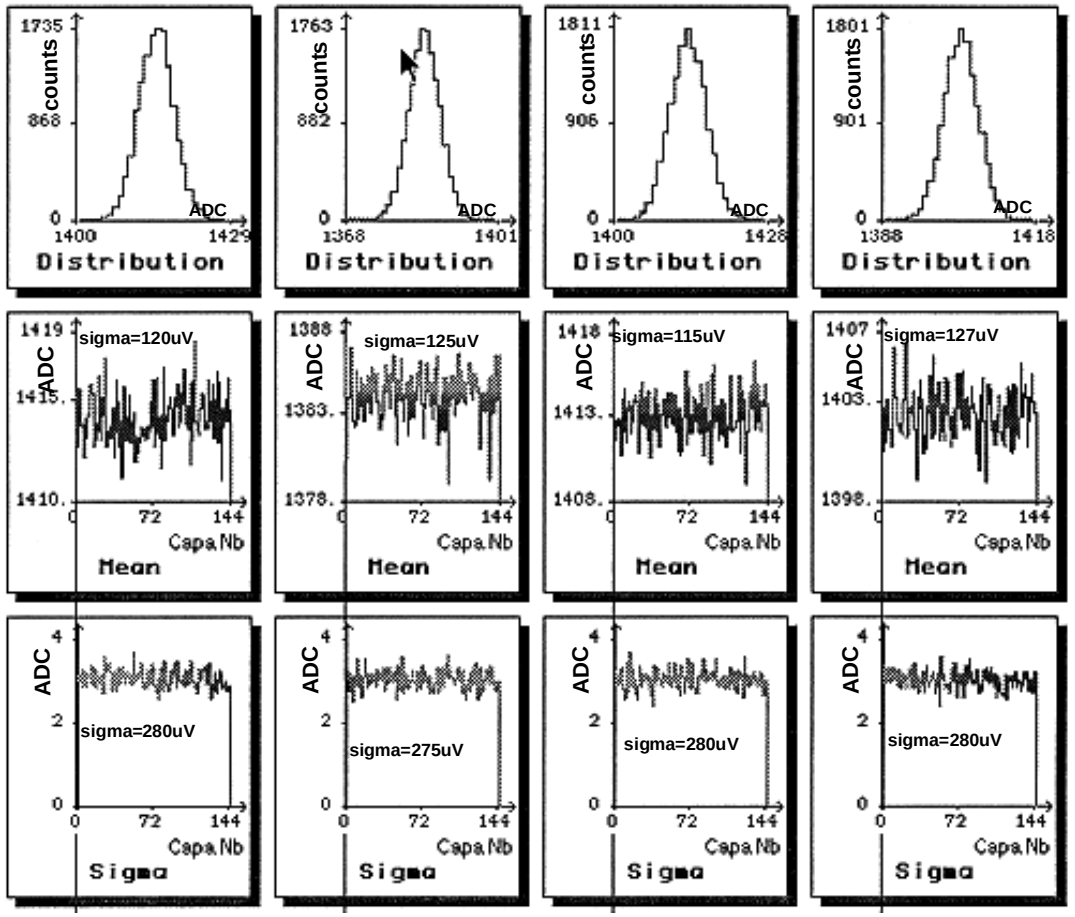


PEDESTAL VALUE
TOTAL DISPERSION
smean(sigma)=360µV

PEDESTAL VALUE
DISPERSION
mean(sigma) =183µV

rms noise
mean(sigma)=303µV

Fig 15.a : noise and fixed pattern noise of 4 channels of a DMILL chip (V1.1)



PEDESTAL VALUE
TOTAL DISPERSION
mean(sigma) =320µV

PEDESTAL VALUE
DISPERSION
mean(sigma)=122µV

rms noise
mean(sigma) =278µV

Fig 15.b: noise and fixed pattern noise of 4 channels of a HP chip

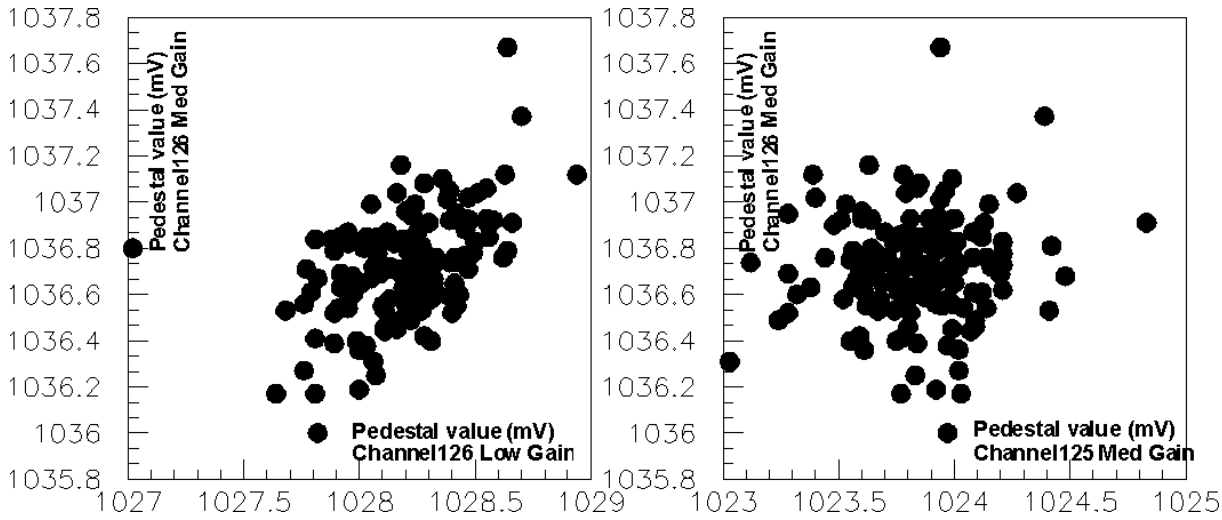


Fig 15.c: Correlation plot of two DMILL SCA channels for two channels sharing the same slave channel and for two channels with different slave channels

The different fixed pattern noise values obtained for the different DMILL batches can not be easily explained by technological parameters.

The figure 16 gives the distribution of the noise and of the fixed pattern noise measured for all the channels of the chips coming from the batch V2 wafer 4.

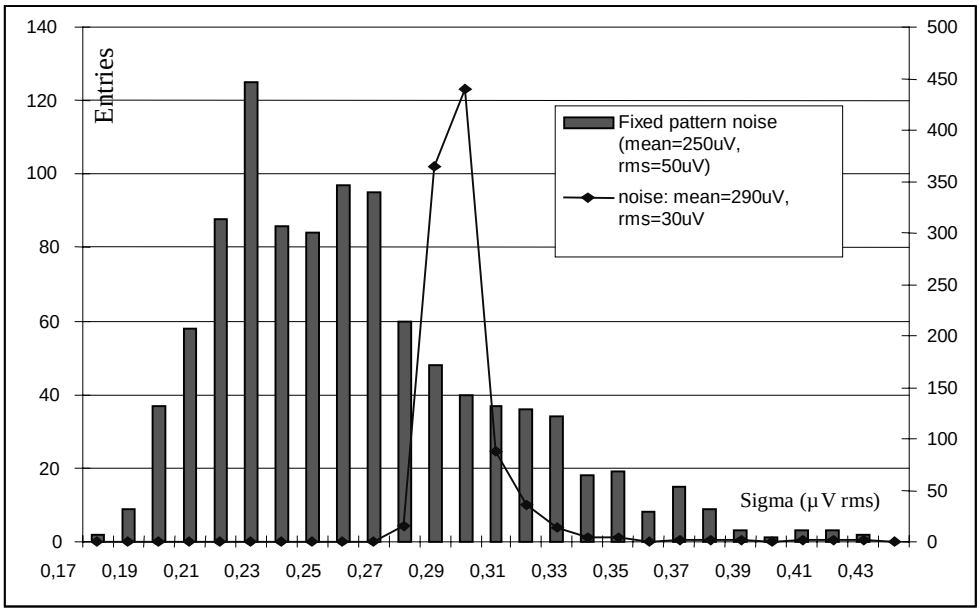


Fig 16 : noise and fixed pattern noise distribution for all the channels of batch V2 W4.

The noise distribution is very narrow, whereas the fixed pattern noise distribution is wider. Similar distributions are obtained for batch V2W12.

The figure 17 shows the effect on a yield of a selection of the chips based on the fixed pattern noise. In this case, a chip is considered bad as soon as the fixed pattern noise of one channel is higher than a threshold.

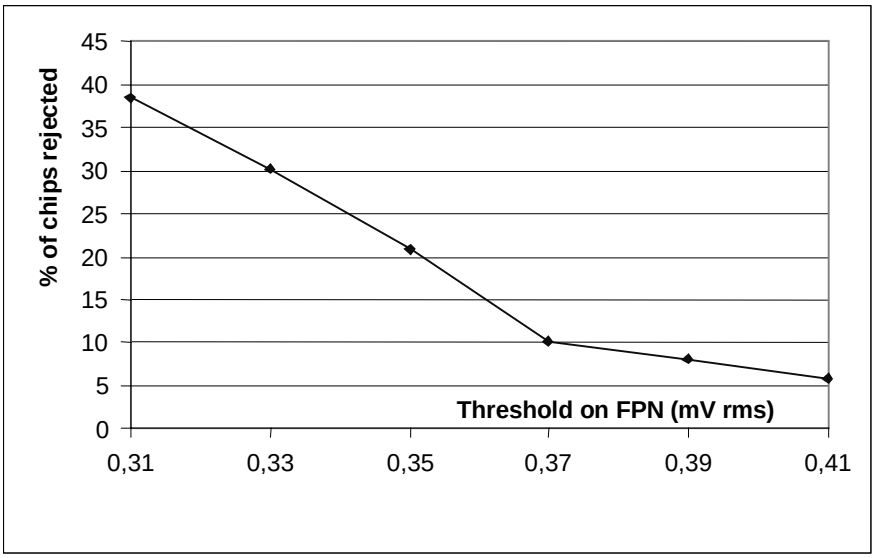


Fig 17 : Effect of selection based on fixed pattern noise on the yield (data from V2W4).

The noise and fixed pattern noise are not impacted by variations of the write amplifier and output buffer bias current by +/- 50%, whereas an increase of the read amplifier bias current decrease slightly the noise.

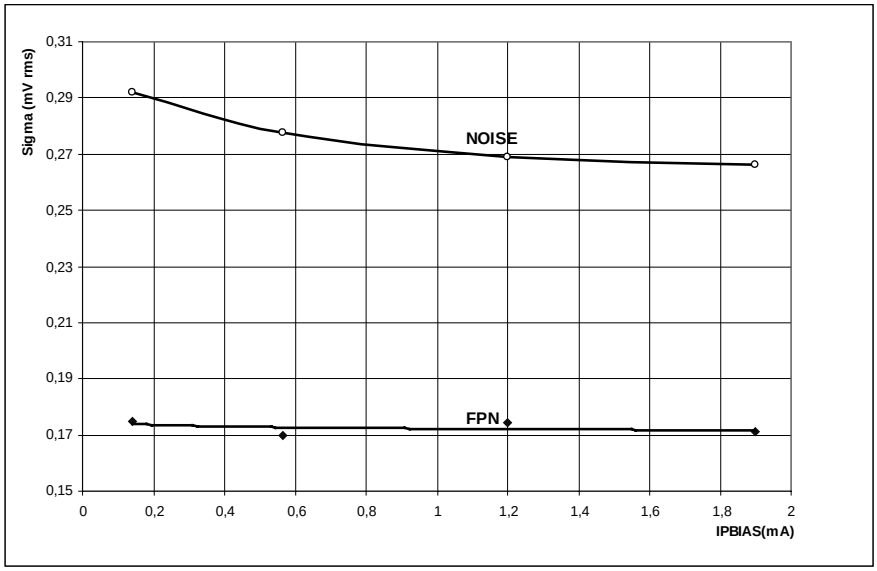


Fig 18 : noise and fixed pattern noise vs read amplifier bias current.

7.5 Other DC measurements.

* Channel to channel offset dispersion can reduce the dynamic range of the system by moving the range of the SCA in respect to the one of the ADC. As the offsets are low, the loss of dynamic range is negligible. These offsets will also pertub the choice of the right gain, because they will appear as gain threshold dispersion between channels and may impose to set a specific gain selection threshold per channel.

	DMILL	HP
Channel Offset dispersion	12mv rms	10mv rms (4chips)

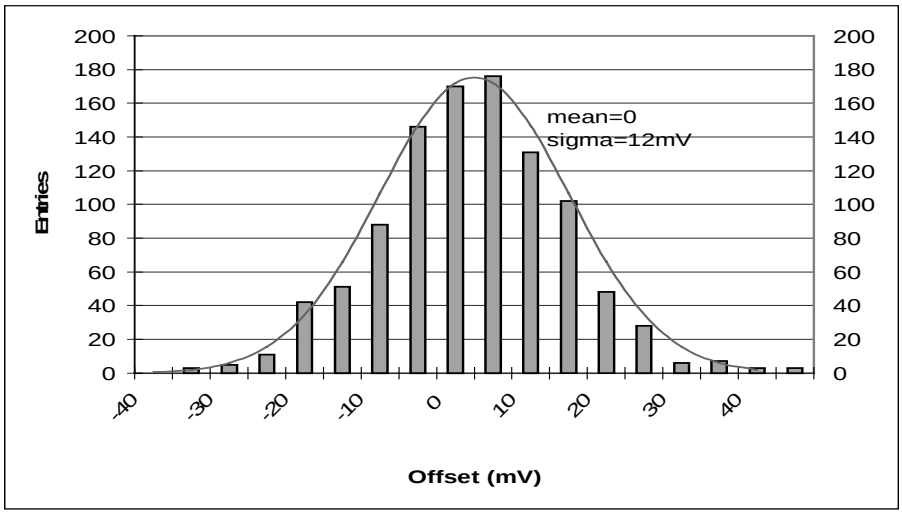


Fig 18 : DC offset distribution (data from V2W4).

* For both the HP and the DMILL versions, the peak-peak cell-to-cell DC gain dispersion is smaller than 0.02%.

7.6 Input Bandwidth, Slew-rate.

The input bandwidth has been measured by sampling sine waves up to 200MHz.
The input Slew-rate has been measured by sampling very fast square waves.

	DMILL	HP
Bwi (INPUT BANDWIDTH)	50MHz	45MHz
INPUT Slew Rate	175V/us	120V/us

The input bandwidth and slew rate are high enough not to distort the shaper signal.
The small difference of bandwidth between the two chips is visible on the figure 20 plot. On this plot the shaper signal has been reconstructed by delaying the calibration pulse in respect to the sampling clock by step of 100ps.

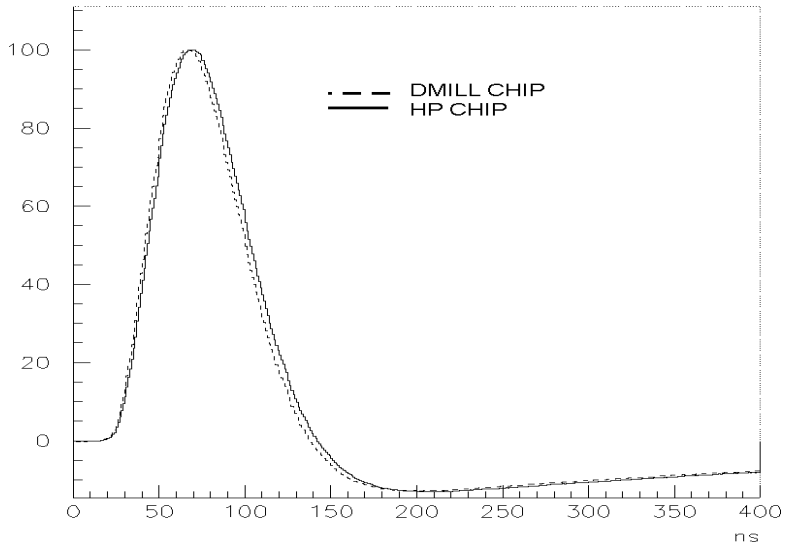


Fig 20 : Same shaper signal sampled on a FEB by a DMILL chip and an HP chip

7.7 Transient Linearity

For all the transient measurement, we used the VME calibration board, a 50 Ohm 0T with a detector capacitance of 680pF and a 3 gain shaper.

Figure 21 shows a typical shaper signal used for the linearity measurement. On this plot, corresponding to a **single shot** acquisition of a medium gain shaper signal, the noise over baseline is smaller than +/-1 mV.

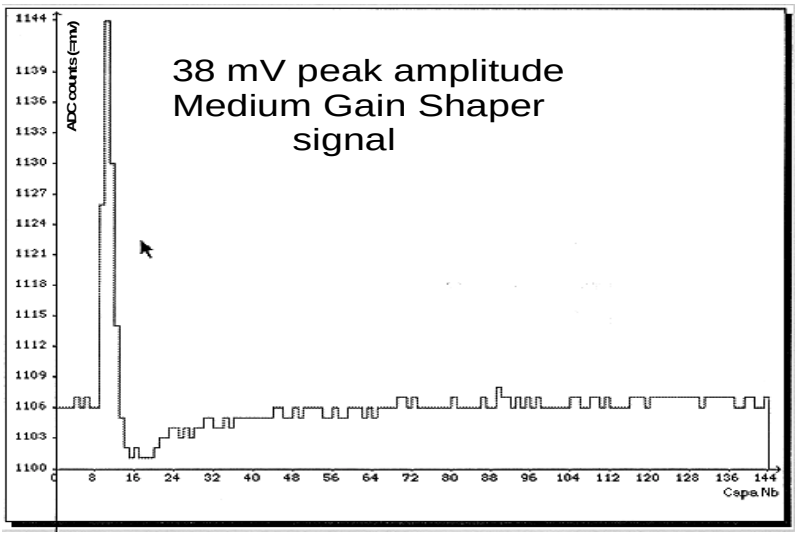


Fig 21: one shot shaper signal sampled by a DMILL chip

The transient linearity has been studied using only for the sample at peak for each of the three gains of the shaper. They were sent successively in the same SCA channel in order to separate the effects of the shaper and of the SCA. The plots of figure 20 to 22 show the residues to linear fit of the overall chain (calibration + 0T + shaper +SCA) for a HP and a DMILL chip. The peak amplitude at the SCA input goes from 0V to 2.9V. The integral non linearity is defined as (data - fit)/max where max, the maximum signal at the SCA input, is considered to be 2.5V. The linearity plots of the two chips are very similar and the non linearity seems to follow the linearity curves of the shaper (Fig15 of LARG Note-No-92).

For high gain and medium gain output the integral non linearity of the chain is better than +/-0.2% in the 0-2.5V range and is probably dominated by the shaper (+ calibration for high gain ?).

For the low gain, the integrated non linearity is better than +/-0.2% in the 0-2.35V range and is still dominated by the shaper.

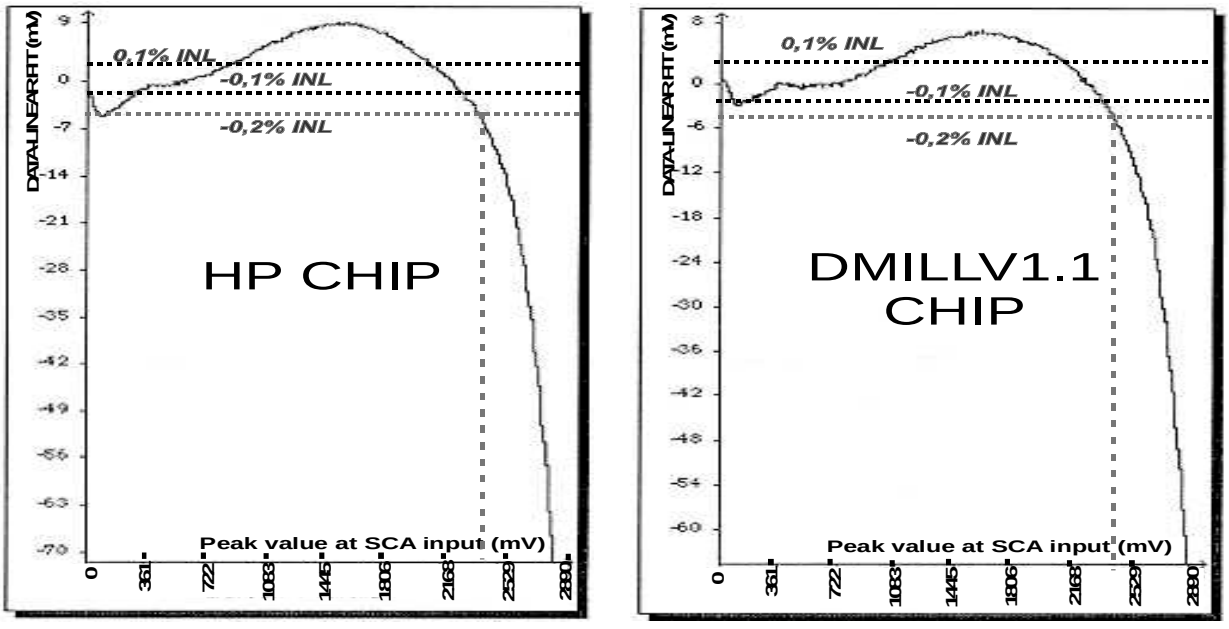


Fig 22a : plots of linear fit residue for low gain shaper

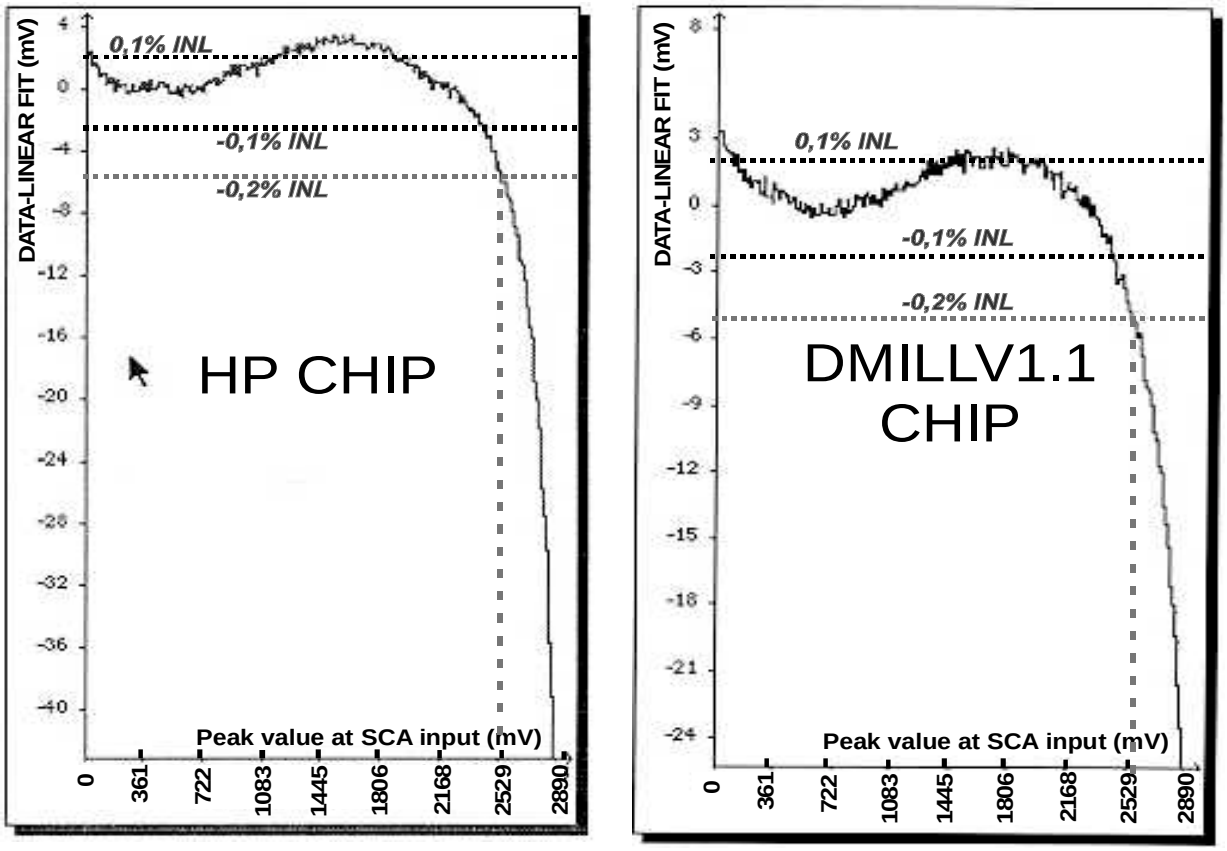


Fig 22b : plots of linear fit residue for medium gain shaper

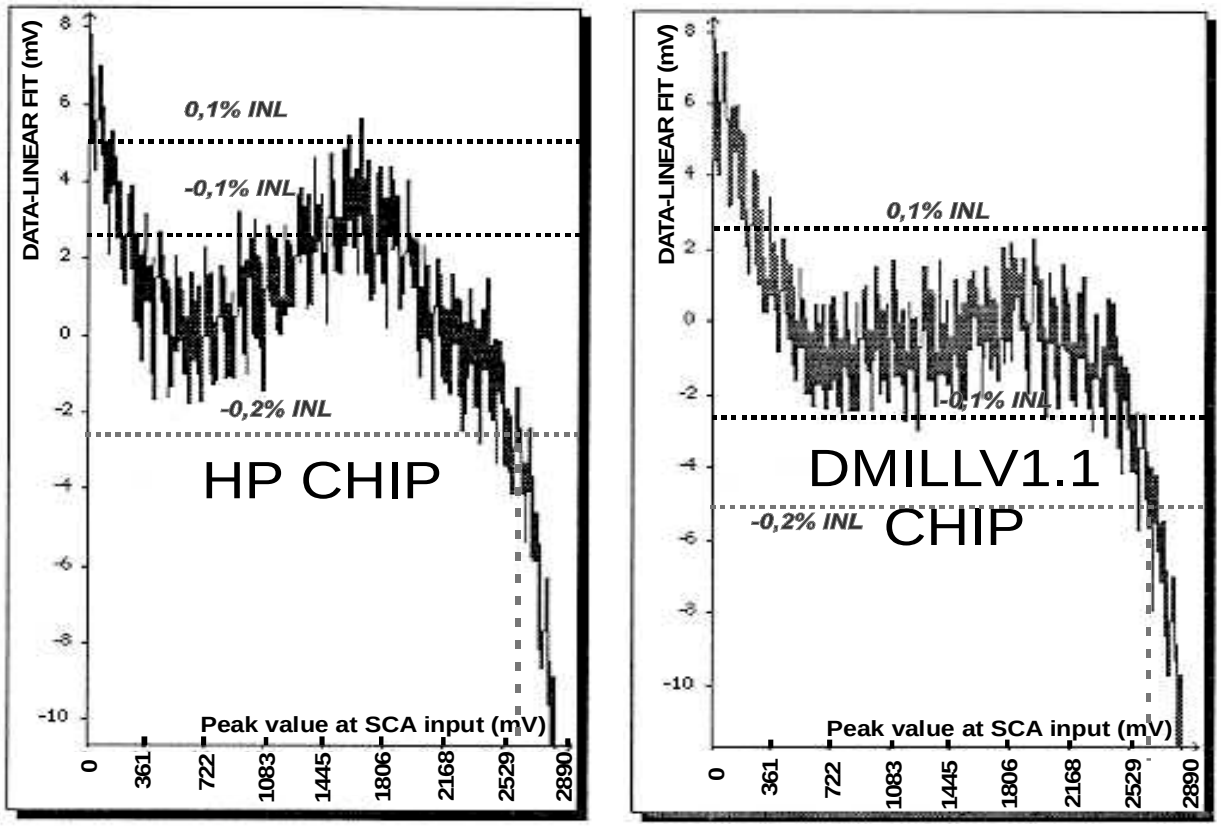


Fig 22c : plots of linear fit residue for high gain shaper

7.8 Multiplexing residue.

Due to the finite bandwidth of the SCA output stage, during the multiplexing operation, the output node of the SCA can keep the memory of a previously multiplexed channel during few tens nanosecond. To study this effect, we have injected a varying DC level in the SCA medium gain channel number 2, while the other channels input voltages are kept to 0V. During the read operation, the 4 medium channels are sequentially (ch1 then ch2 then ch3 then ch4) multiplexed at the nominal **5Mhz** rate, and the multiplexing residue is measured on the 3rd medium gain channel (after pedestal subtraction). This measurement is dependant of the value of the (parasitic) capacitance connected at the output of the SCA. On the Orsay test setup (with only SCA mounted),

the measured residue **MUXRES = 1^{E}-4** of the previous multiplexed value.

7.9 DC cross-talk

A DC cross-talk in the chip is possible due to parasitic capacitance between the read top and read bottom bus of adjacent channels. This effect has been studied using the same method than multiplexing residue. No visible effect has been seen.

DC-XTALK < 1^{E}-4

7.10 Transient cross-talks.

Whereas DC-cross-talk are due to parasitic effects in the read-out and multiplexing part of the circuit, the transient cross-talk are more referred to its input section. The measurement of this type of cross-talk is very difficult on the test-bench, where couplings are dominated by effects on the board or the socket. To measure it, one input is fed by a shaper signal,, synchronous of the write address sequence, while all the other input pins are grounded directly on the SCA socket. A x11 gain is put in front of the ADC, and fixed pattern noise and noise are reduced by cell by cell pedestal subtraction and averaging.

Fig 22 shows the results on H1 and L1 channel for a signal send in channel M1. The signal, shaped as on FIG 19), send on M1 presents a peak value of 2.2V. The calibration board is synchronized with the write addresses so that the peak of the signal is always located on cell 10. A cross-talk signal is seen on channel H1 but not in L1.

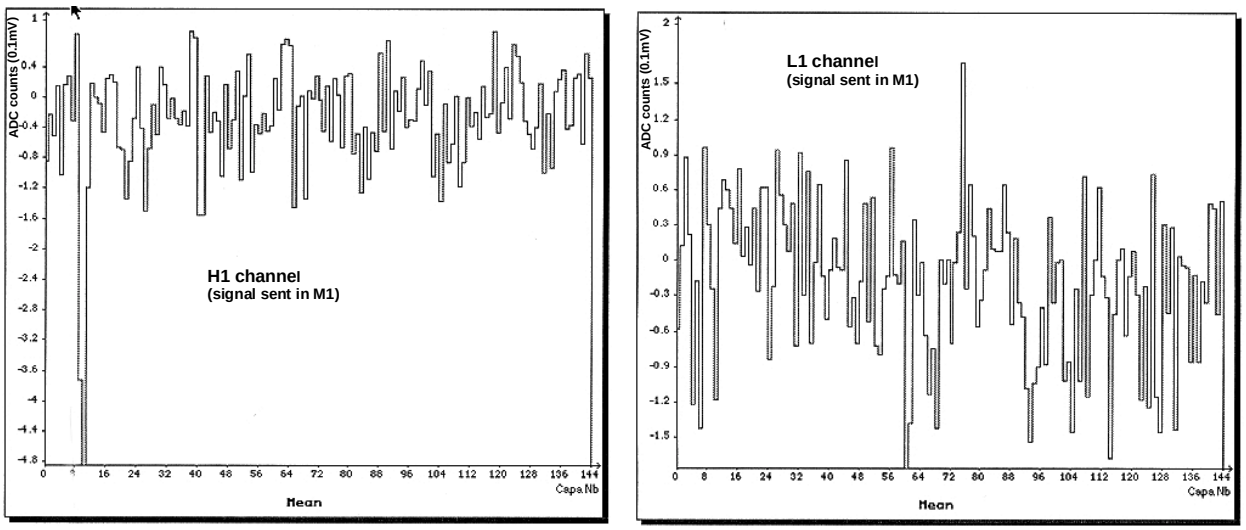


FIG 22 : cross-talk from channel M1 to H1 and L1 (2.2V peak shaper signal on M1)

The following table summarizes the transient cross-talk measurements performed :

'Receiver'	***Hi***	***Mi***	***Li***	***Channel from an other group***
'Source'				
Hi		**$< 1^{E}$-4**	**$< 1^{E}$-4**	**$< 1^{E}$-4**
Mi	**= -2.5^{e}-4 of the input signal (same shape inverted)**		**$< 1^{E}$-4**	**$< 1^{E}$-4**
Li	**$< 1^{E}$-4**	**$< 1^{E}$-4**		**$< 1^{E}$-4**
Channel from an other group	**$< 1^{E}$-4**	**$< 1^{E}$-4**	**$< 1^{E}$-4**	

All these cross-talks are negligible when compared to those obtained in the shaper.

7.11 Memory cell 'remanence'.

Between two successive write operations in the same cell, the latter is not reset. A storage cell can indeed keep a residue of the value which was previously stored on it. This effect is called memory cell remanence (**MCREM**).

To measure this effect, a shaper signal is stored on the SCA, then immediately overwritten by a baseline signal. The resulting signal is then read-out.

	HP	DMILL V1.1
MCREM (fraction of the previously written signal)	-0.2%	-0.07%

This effect is visible in simulations and is due to the behavior of the write amplifier when a pre-charged capacitor is switched on at its output.

The effect of this limitation on the overall resolution has to be studied.

7.12 Sampling time accuracy.

The accuracy of high dV/dT signal measurement is impacted by the precision of the sampling time. The reproducibility of the sampling time for one given cell will be called the sampling time jitter. Another source of sampling time error will be the cell-to-cell sampling time dispersion.

To measure this effect, a high dV/dT signal, synchronous with the write-clock, is sent to the SCA. Practically, this signal is a high amplitude shaper signal, and the 2nd sample (within the positive slope of the signal) is the one studied. The slope (dV/dT) of this signal is measured by delaying it by +/- 0.5ns.

The sampling time jitter (**stj**) will be calculated as the ratio of the excess noise on a given cell over the slope of the signal. This excess noise is defined as the quadratic difference between the noise measured with the transient signal at input and the one measured with a static signal at input. For the two chips, this measurement leads to :

stj =45 ps rms

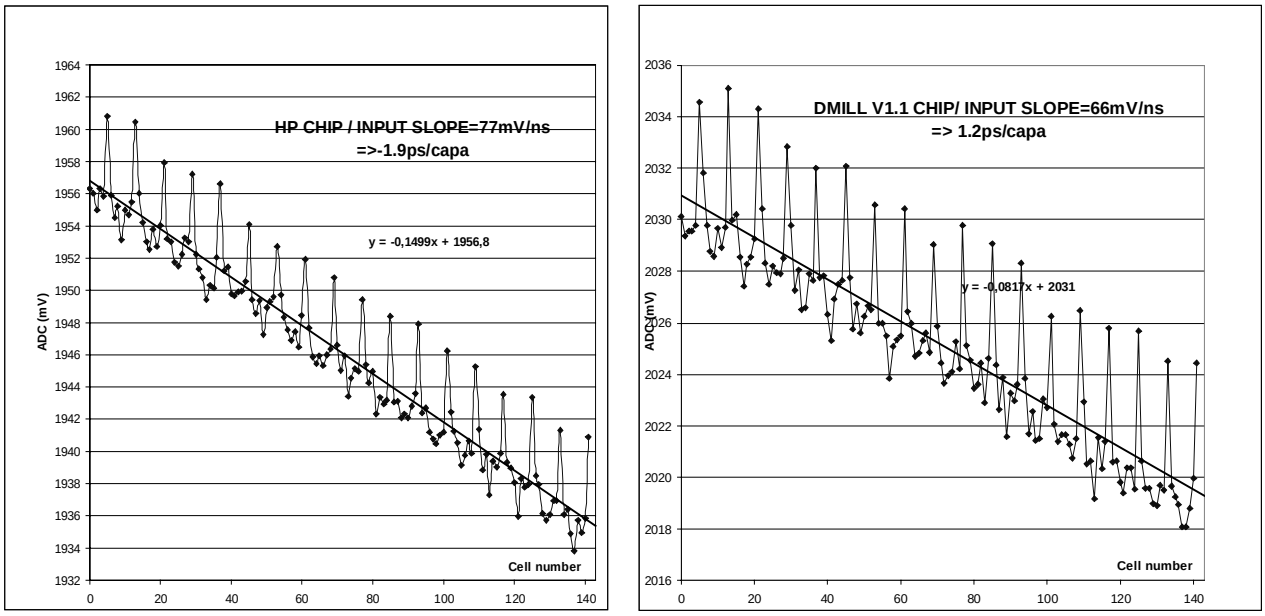


Fig 23 : cell to cell voltage dispersion for a high dV/dT signal sampled inside the SCA (standard addressing arrangement)

The precision of this measurement is limited by the jitter between the calibration signal and the write clock. A more accurate measurement performed by sampling the write clock itself on the very first prototype of the HP chip gave **stj =9 ps rms**

The cell-to-cell sampling time dispersion is calculated by the ratio of the cell-to-cell sampling voltage dispersion over the slope of the signal.

From this evaluation, it comes that the sampling time variation with the storage cell number is quasi-linear : the sampling in the last cell will be sooner than in the first one.

The measured cell-to-cell sampling dispersion is :

	HP	DMILL V1.1	DMILL V2
Cell-to-cell sampling time dispersion	280 ps peak-peak	172ps peak-peak	180ps peak-peak

This effect also seen in simulation is due to the parasitic resistor of both the write bus and the write-clock bus. Indeed, these two busses present distributed present capacitor and resistor which act as delay lines for the clock and the input signal (around 1.5ns along the chip). As the delay is not exactly the same on the two busses, the two signals will loose their relative phase along the chip.

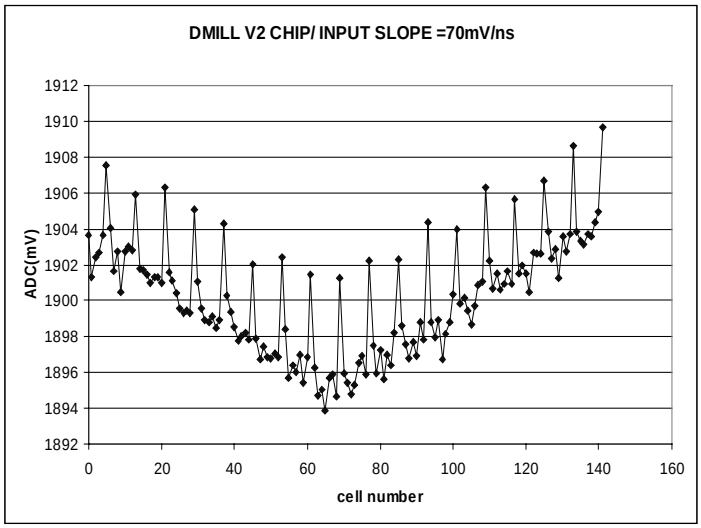


Fig 24 : cell to cell voltage dispersion for a high dV/dT signal sampled inside the SCA (DMILL V2 : modified addressing arrangement)

This effect is very small if we consider that the 5 samples of a same event are stored in adjacent cells, but may be not negligible if not : for instance, if the event is stored in the cells 142, 143, 0, 1, 2.

To avoid this edge effect, the write and read address decoders of the V2 chip have been modified so that:

- the grey code 0 address the 1st physical column of the chip
- the grey code 1 address the 3rd physical column of the chip.
- the grey code n (n<=71) address the 2n+1 physical column.
- the grey code 72 address the last column
- the grey code n (143>n>72) address the 288-2*n column
- the grey code 143 address the 2nd physical column of the chip

The effect of this modified decoding is plotted on fig 24 for experimental conditions equivalent to those used for fig 23:

- the overall cell-to-cell dispersion is the same as for the standard decoding.
- The time-vs-capacitance address slope is doubled, but the 144-0 edge effect disappear.

The modulo 8-pattern appearing on the fig 23 and fig 24 plots is not yet explained. Its amplitude is proportional to the dV/dT slope of the input signal and is comparable for the HP and DMILL chip. Such a pattern could be due to an address-dependent sampling time skew, but simulations can not put in evidence such a skew. This effect, not seen on Nevis test bench may come from the test bench.

7.13 Voltage droop-rate.

The voltage droop rate is the rate corresponding to the discharge of the storage capacitance due to leakage of the MOS switches. For a 2V signal stored in the capacitor, the droop rate is smaller than **250µV/460µs** (which is the minimum value measurable with the test bench) for the two technologies.

8 IRRADIATION TEST RESULTS.

Although the HAMAC chip is manufactured on DMILL rad-HARD technology which is guaranteed by TEMIC-MATRA MHS for 10 Mrad total dose and 10^{14} Neutrons/cm^2 integrated fluence, irradiation tests have been performed on the chips.
For the two types of irradiation, the following data have been measured before and after irradiation.

-power consumption.
-mean pedestal value.
-fixed pattern noise.
-noise.
-DC range.
- transient behavior.

During all the irradiations, the circuits are working. The 40 Mhz write operation as the read operation are sequenced by a board located outside the irradiation facility. The analog outputs of the chips are available for monitoring.

8.1 Gamma irradiation test.

Three samples of the HAMAC chip have been irradiated up to 300 krad SiO2. The irradiation was performed at the Cocase (Saclay) gamma irradiation facility using a Co^{60} source. The dose rate used was 140rad/h. The chips were tested within a day after the irradiations.

a/ Chips irradiated.

The following chips have been irradiated :

- E1-16 and E1-18 from batch V1.1
- E3-0 from batch V1.2

At the end of the irradiation the chips are still fully functional.

b/ Power consumption.

Fig 25 gives the evolution of the power consumption with dose. This evolution stays smaller than the 1 mA accuracy of the test setup.

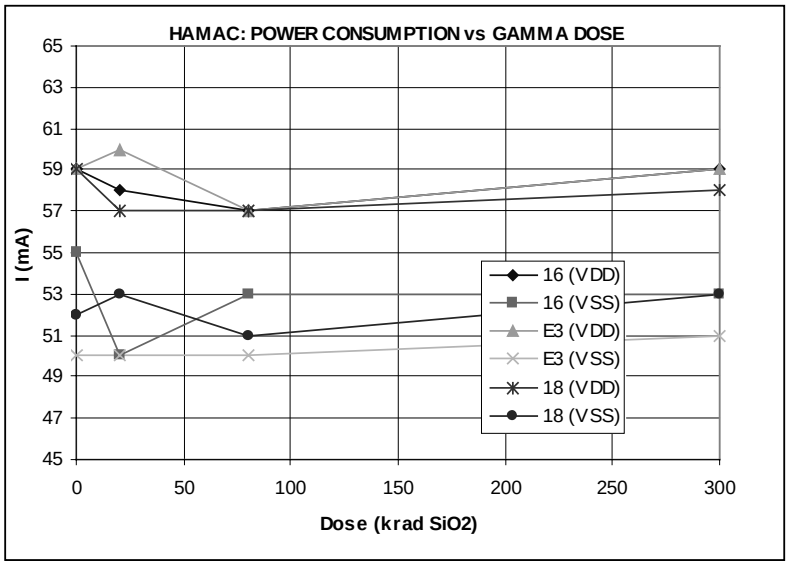


Fig 25: power consumption variation with gamma irradiation.

c/ Pedestal shift.

Fig 26 shows the pedestal value shift with gamma irradiation for all the SCA channel tested. This shift is small but its value is not 0 . The mean value over all the channels of this shift is zero.

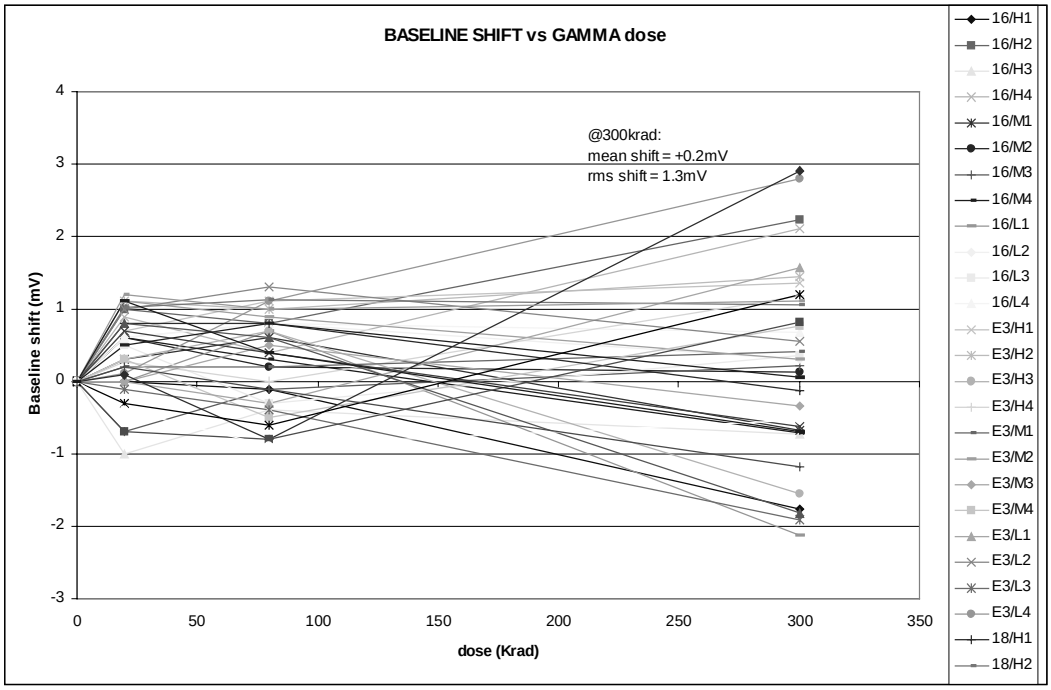


Fig 26: baseline shift with gamma irradiation for the 36 tested channels.

d/ Fixed pattern noise.

The evolution of the fixed pattern noise with dose up to 300 krad is negligible. The Fig27 shows this evolution for the mean value of the fixed pattern noise of each chip.

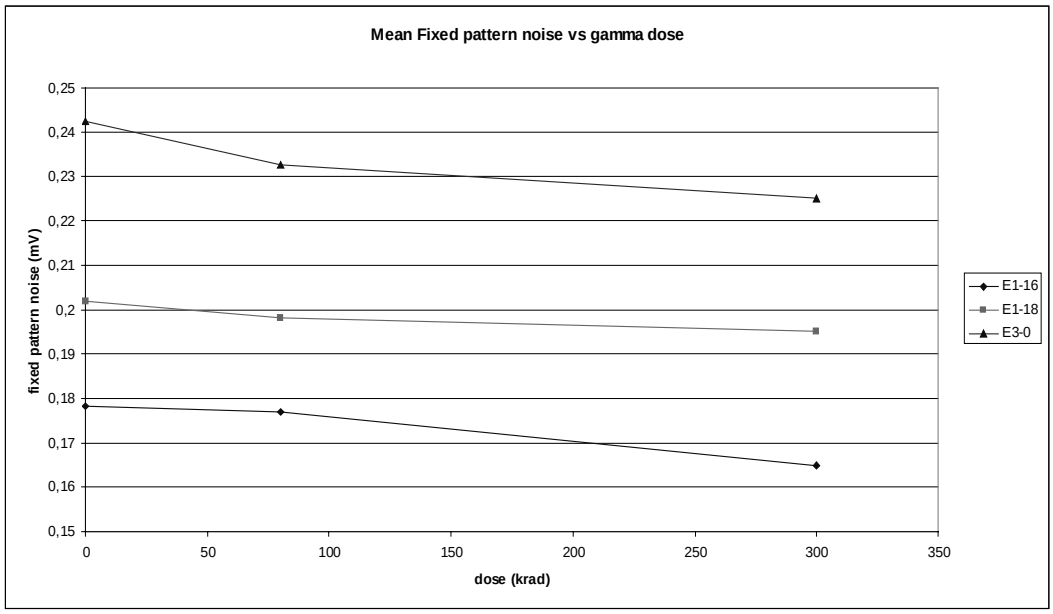


Fig 27: mean fixed pattern noise evolution with gamma irradiation

e/ Noise.

The evolution of the noise (plotted on figure 28) with dose up to 300 krad remains also negligible

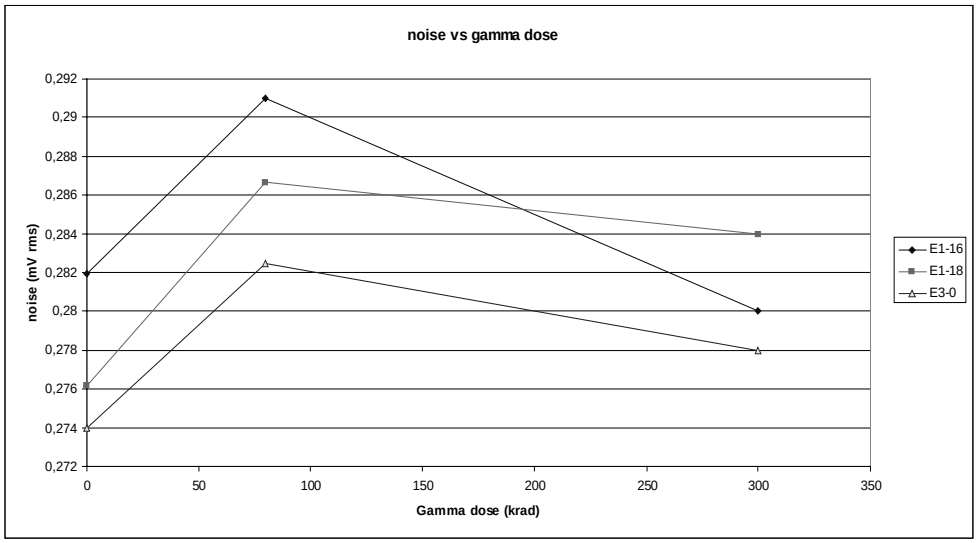


Fig 28: mean rms noise evolution with gamma irradiation

f/ Voltage droop rate.

The voltage droop rate may change after irradiations because of possible current leakage appearing on NMOS switches.
After a 300 krad irradiation, the voltage droop rate remains unchanged smaller than 250µV/460µs.

8.2 Neutron irradiation.

Neutron irradiations up to 3.10^{13} neutrons/cm^2 (+/- 40%) have been performed in the CERI facility (Orleans) in June 1999. Taking into account the facility energy spectrum [11] , this fluence is equivalent to a $4.5\ 10^{13}$ N/cm^2 irradiation with 1MeV Neutron.

The chips were tested only after 2 months, period necessary to reach back a reasonably low radioactive activity.

a/ Chips irradiated.

The following chips have been irradiated :

- E1-15 and E1-17 from batch V1.1
- E3-1 from batch V1.2
- E3-1 from batch V2.w12

At the end of the irradiation the chips are still fully functional.

b/ Power consumption.

Fig 29 gives the evolution of the power consumption with neutron irradiation. This evolution stays smaller than the 1 mA accuracy of the test setup.

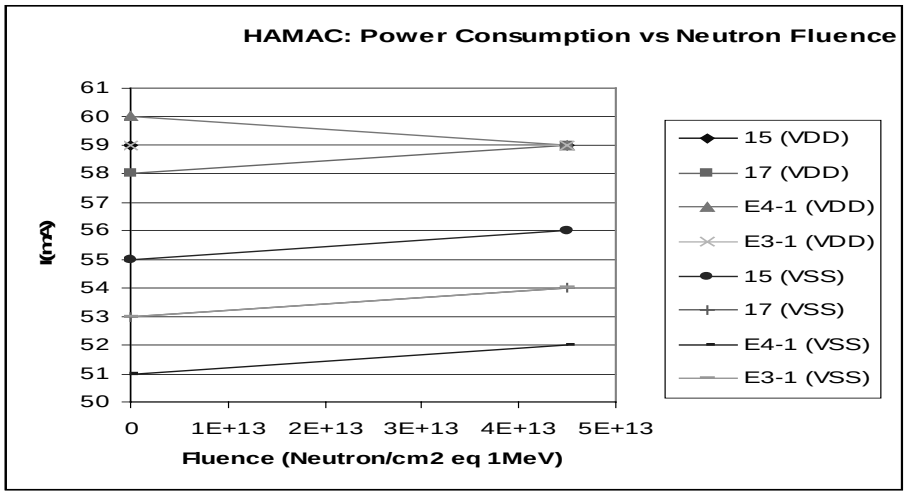


Fig 29: power consumption variation with gamma irradiation.

c/ Pedestal shift.

Fig 30 shows the pedestal value shift with neutron irradiation for all the SCA channel tested. This shift is small but its value, as for gamma irradiation is not 0 . The mean value over all the channels of this shift is zero.

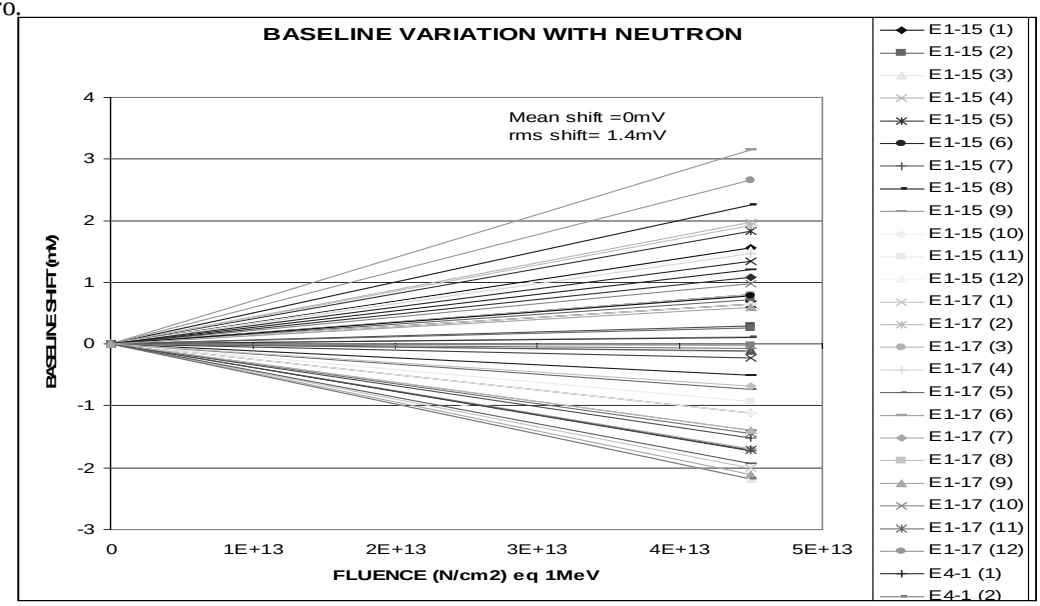


Fig 30: baseline shift with gamma irradiation for the 48 tested channels.

d/ Fixed pattern noise.

The evolution of the fixed pattern noise with neutron irradiation is negligible. The Fig31 shows this evolution for the mean value of the fixed pattern noise of each chip.

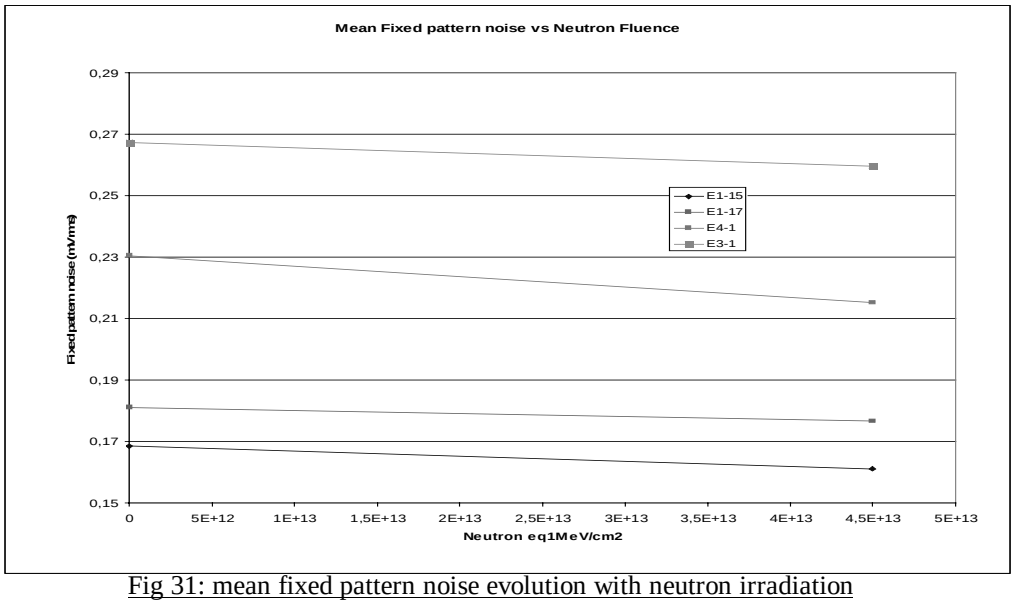


Fig 31: mean fixed pattern noise evolution with neutron irradiation

e/ Noise.

The evolution of the noise (plotted on figure 32) with neutron irradiation remains also negligible.

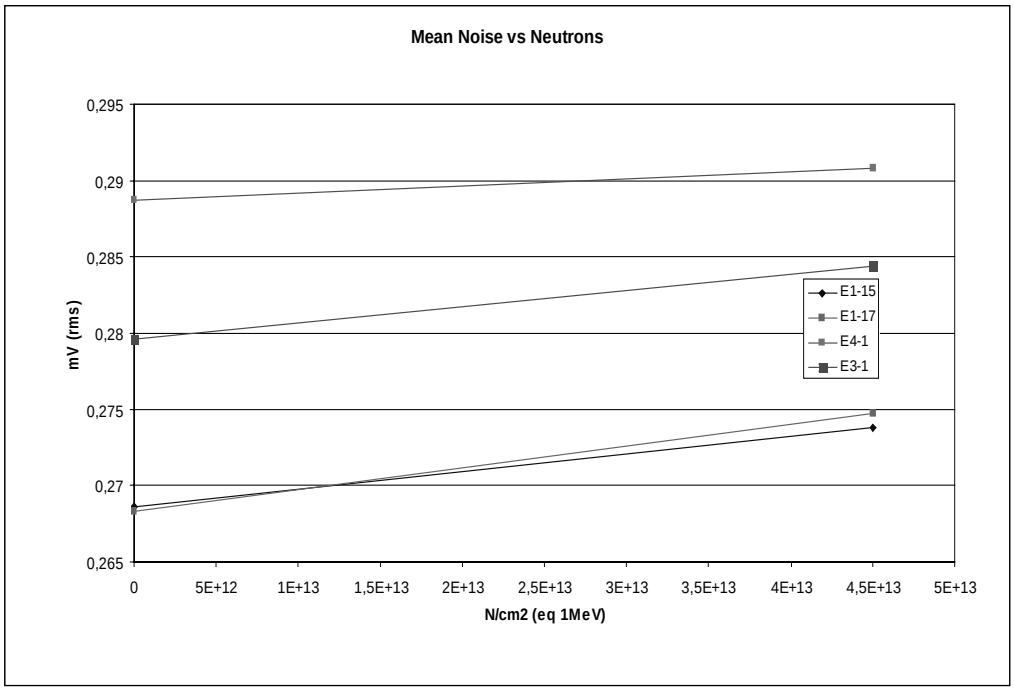


Fig 31: mean rms noise evolution with neutron irradiation

f/ Voltage droop rate.

After the $4.5^{E}13$ N/cm^2 irradiation, the voltage droop rate remains unchanged smaller than 250µV/460µs.

9 POSSIBLE CHANGES FOR THE PRE-PRODUCTION PROTOTYPE.

Minor changes are possible or necessary before submitting the pre-production prototype:

9.1 Width of the clock lines.

On the existing chips, the width of the clock lines of the write and read decoder (see2.3.3) is 1.4µm (metal2). Taking into account the long term reliability rules concerning electromigration for transient current, this width should be at least 1.6um . In the pre-production run, these lines will be widened to 2µm.

9.2. Bulk Connection of the “return” source follower buffer

This modification is explained in 5.2. It is easily feasible in the present layout.

9.3 Current limitation in the input protections.

The NMOS input protections used in the chip (see3.3) does not have any current limitation.
16 SCAs share the same address bus. If one address input of one SCA is internally short-circuited to vss or vdd, the corresponding bit will be shorted to the same potential for the 16 SCAs.
If the positive power supply of the (PECL) circuits buffering the address lines is set before the one of the SCAs, the NMOS protections will be ON, flowing then a high current which can damage the PECL buffers. This is not the case on the actual design of the Front End board where these buffers and the SCAs have a common voltage regulators.

For this reason, the feasibility of adding a current limiting resistor in serie between the pad and the anti-ESD protection is under study and in particular its impact to the timings. This limiting resistor would be a few hundred ohms diffusion (DSP) resistor. Its layout is already qualified by MHS and its small dimension allow to add it on the present layout without any difficulties.

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[9] R.Bernier et al, "SPAC : Serial Protocol for the Atlas Calorimeter", ATLAS LARG internal note ATLAS-AL-LAL-ES-9.0

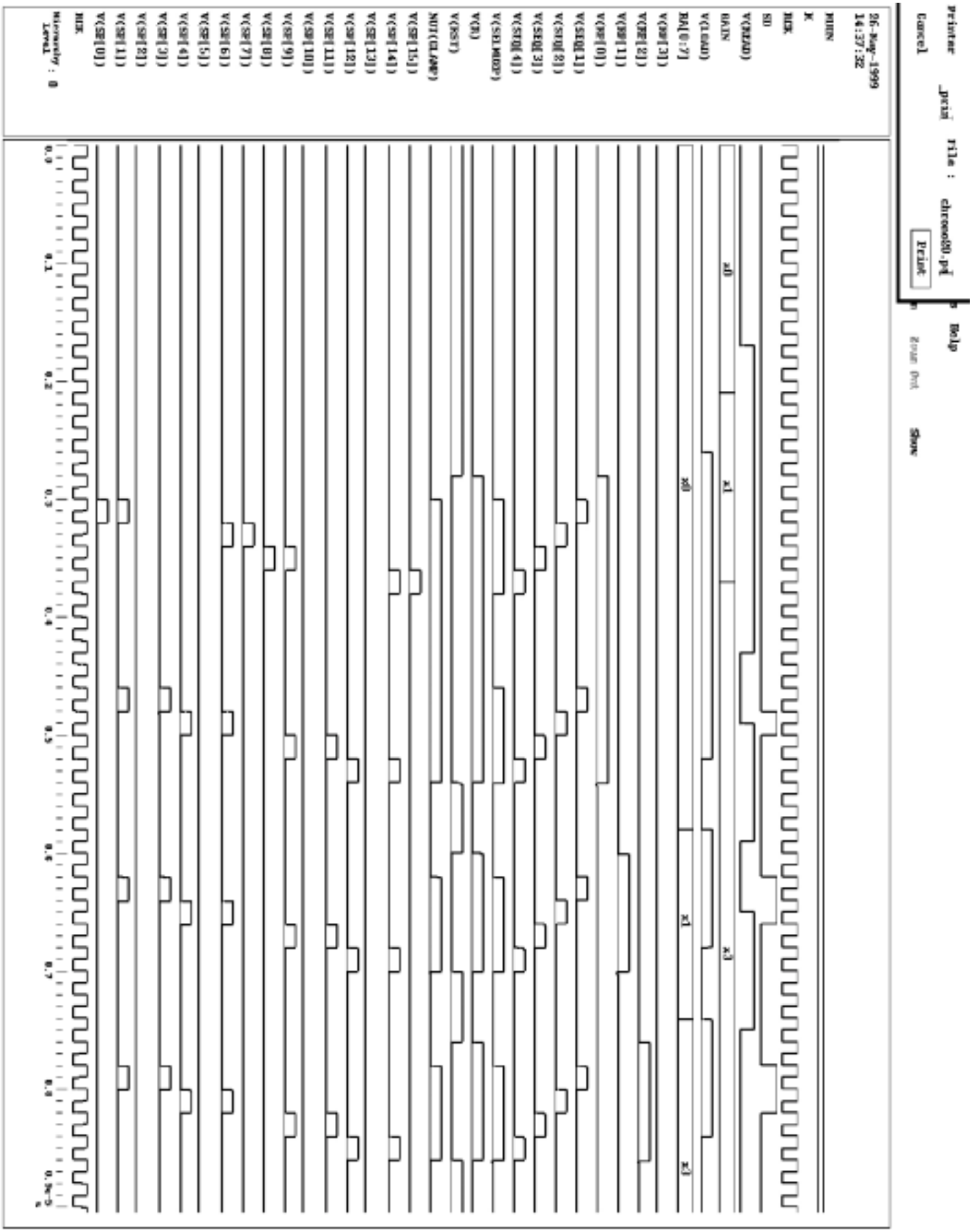
[10] J. Kaplon, CERN, private discussion.

[11] J. Collot et all, " A NEUTRON IRRADIATION FACILITY FEATURING CRYOGENIC TEMPERATURES AND DEDICATED TO LARGE HADRON COLLIDER DESIGN", NIM A350 (1994) 525-529

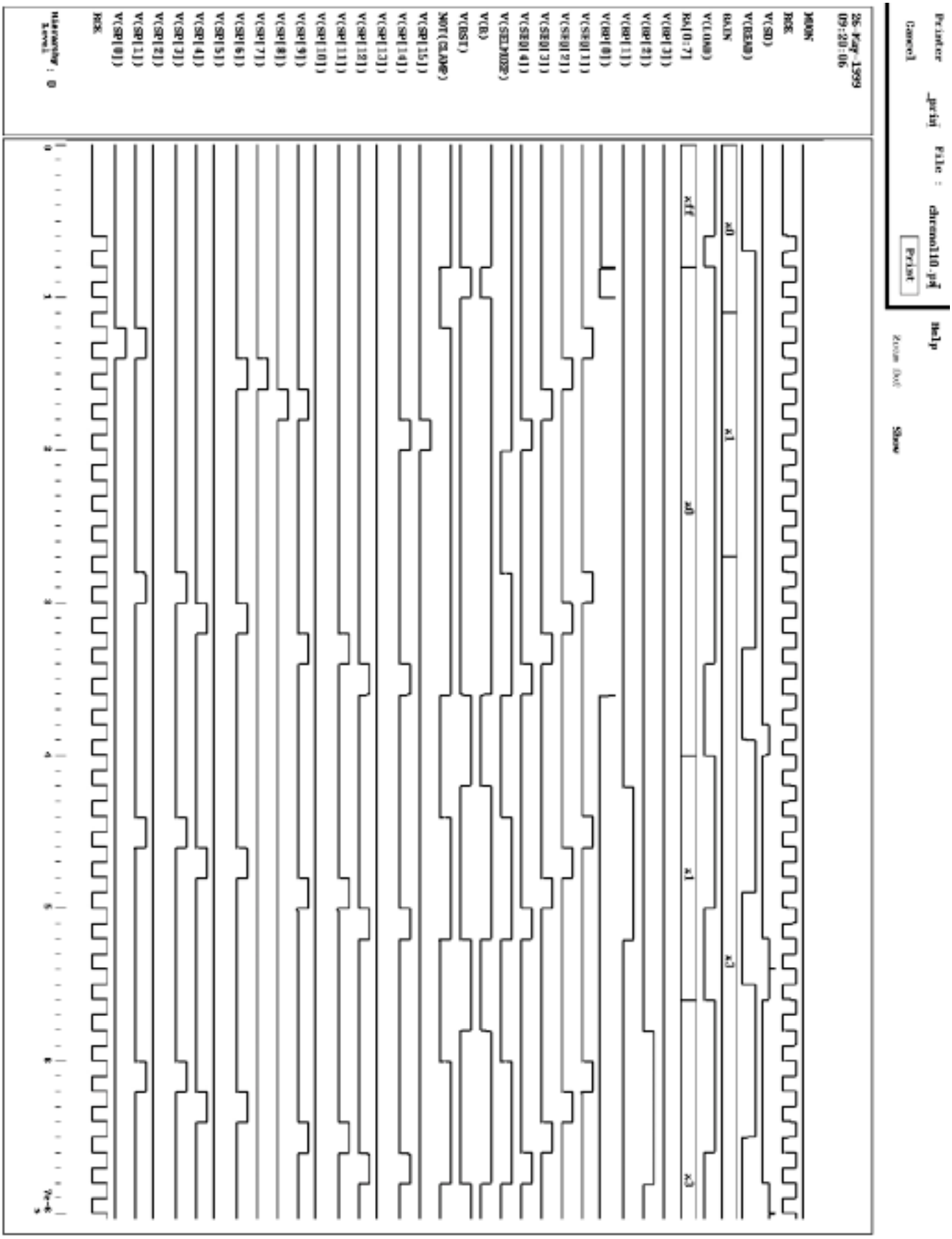
APPENDIX I

SIMULATED
TIMING DIAGRAMS OF
THE READ-OUT OPERATION

MUON=0 M=1. Gain Selection on the first sample, then reading of two other samples:



MUON=0 M=0. Standard Gain Selection on the first sample, then reading of two other samples.



MUON=1 M=0, reading of the 12 channels for 3 samples.